P1010RDB-PB Hardware User Guide

P1010RDBPBUG
Rev. 0, 09/2013

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Chapter 1
P1010RDB-PB: Overview

1.1 Introduction

The reference design board (RDB) is a system featuring the P1010E/P1014E rev2.0 QorIQ processor, which includes a built-in security accelerator. This low-cost, high-performance system solution consists of a printed circuit board (PCB) assembly and a software board support package (BSP). This BSP enables the fastest possible time-to-market for development or integration of applications including printer engines, broadband gateways, no-new-wires home adapters/access points, and home automation boxes.

This document describes the hardware features of the board including specifications, block diagram, connectors, interfaces, and hardware straps. It also describes the board settings and physical connections needed to boot the RDB. Finally, it considers the software shipped with the platform.

When you finish reading this document, you should be familiar with:

- Board layout and its interfaces
- Board configuration options
- How to get started and boot the board

This document is applicable for 700-27904 RevA or larger. The revision information is shown in the label at the top of the board.

This figure shows an overview of the P1010RDB-PB board details

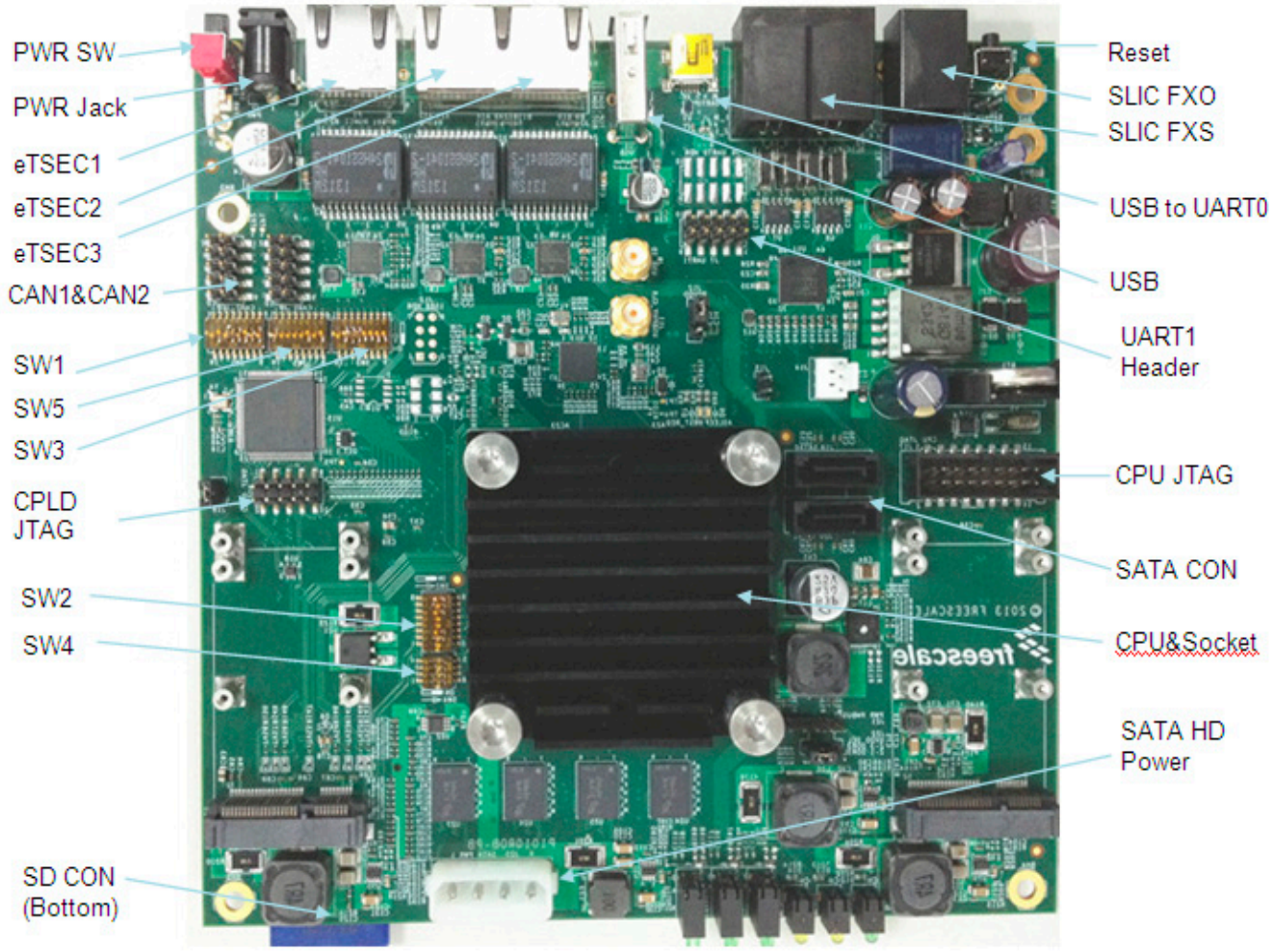

Figure 1-1. P1010RDB-PB Board Details

1.2 Acronyms and Abbreviations

This table lists commonly used acronyms and abbreviations.

Table 1-1. Acronyms and Abbreviations

COP	Debug Port in Powerpc	**PHY**	Physical Layer Interface Device
DDR	Double Data Rate DRAM	**PLL**	Phase Lock Loop
HSSI	High Speed Serial Interface	**SERDES**	Serializer/Deserializer
PCIe	PCI Express®	**USB**	Universal Serial Bus

1.3 Reference Documents

Freescale documentation is available from the sources listed on the final page. Some documents may be available only under a non-disclosure agreement (NDA). For those documents, contact your local field applications engineer or sales representative to obtain a copy.

- *QorIQ P1010E Integrated Processor Reference Manual*
- *QorIQ P1010E Integrated Processor Hardware Specification*

Chapter 2
RDB Hardware

2.1 Overview

This section covers the features, block diagram, specifications, and mechanical data of the RDB.

2.2 Features

The board features are as follows:

- P1010E running at 1000 MHz, platform 400 MHz, DDR3 800 MHz data rate.
- Memory subsystem:
  - 1Gbyte unbuffered DDR3 SDRAM discrete devices (32-bit bus)
  - 32 Mbyte NOR flash single-chip memory
  - 2 Gbyte NAND flash memory
  - 256 Kbit M24256 I2C EEPROM
  - 16 Mbyte SPI memory
  - 1 Kbit I2C Board EEPROM memory
  - 4 Kbit I2C SPD memory
  - SD/MMC connector to interface with the SD memory card
- Interfaces:
  - PCIe:
    - Lane0: x1 mini-PCIe slot
    - Lane1: x1 mini-PCIe slot
  - SATA:
    - 2 internal SATA connectors
  - 10/100/1000 BaseT Ethernet ports:
    - eTSEC1, RGMII: one 10/100/1000 port using Qualcomm Atheros® AR8033
    - eTSEC2, SGMII: one 10/100/1000 port using Qualcomm Atheros® AR8033
    - eTSEC3, SGMII: one 10/100/1000 port using Qualcomm Atheros® AR8033
  - USB 2.0 port:
    - x1 USB2.0 port: connected via an internal PHY to typeA connector
  - FlexCAN ports:
    - x2 DIP headers for FlexCAN bus (revision 2.0B) interface;
  - DUART interface:

  - UART0 interface: supports UART0 to 115200 bps console display via USB to RS232 convertor
  - UART1 interface: support RS232 via a DIP header.
- TDM
  - 2 FXS ports connected via an external SLIC to the TDM interface. SLIC is controlled via SPI.
  - 1 FXO port connected via a relay to FXS for switchover to POTS

- Board connectors:
  - Power supply barrel connector
  - JTAG/COP for debugging
- IEEE Std. 1588® signals for test and measurement
- Real-time clock on I^2C bus
- POR
  - support critical POR setting changed via switch on board
- PCB
  - 6-layer routing (4-layer signals, 2-layer power and ground)

This figure shows the P1010RDB-PB block diagram.

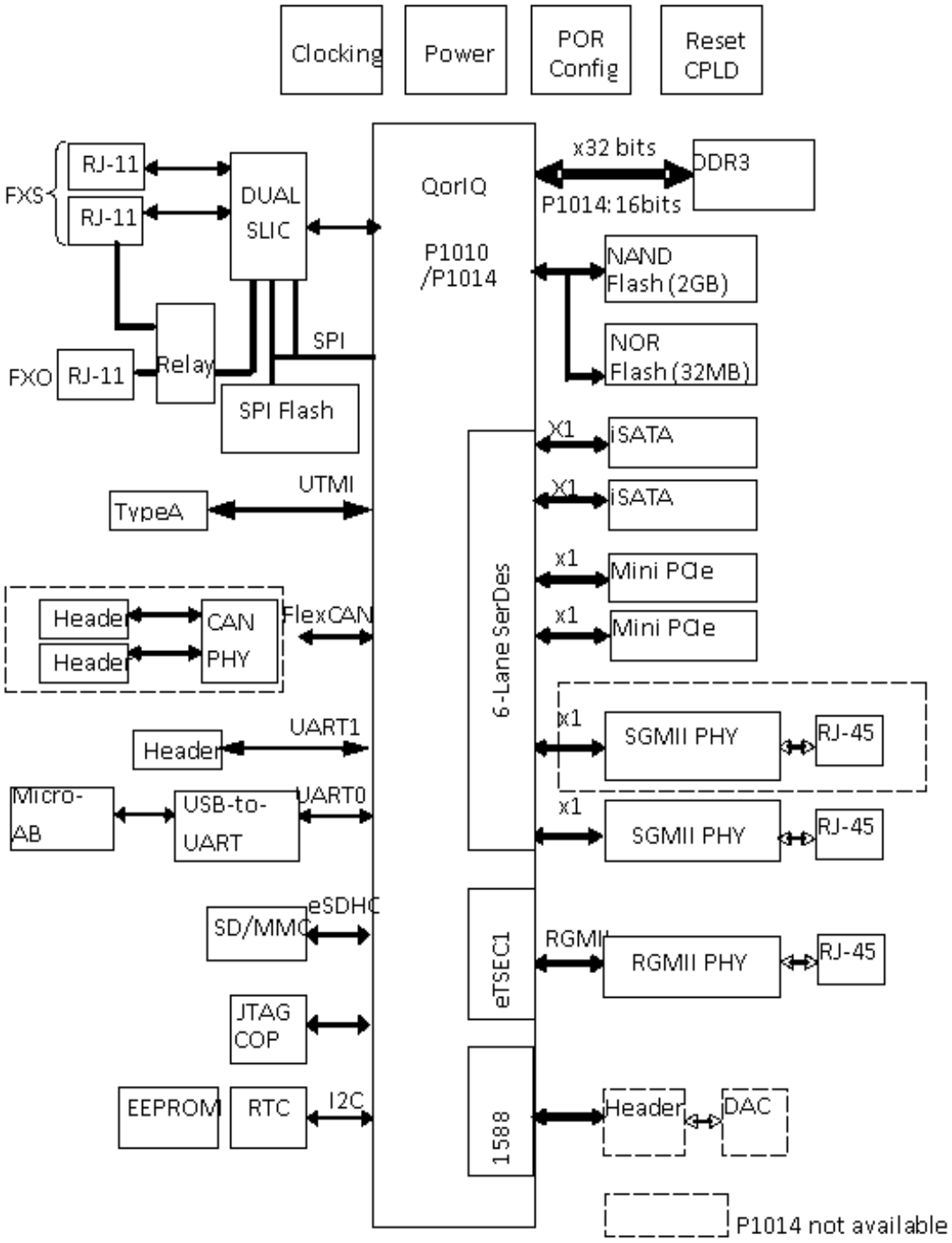

Figure 2-1. High Level Block Diagram

2.3 Specifications

This table lists the specifications of the P1010RDB-PB.

Table 2-1. RDB Specifications

Characteristics	Specifications
Chassis Power requirements	Typical Maximum 60 W 12 V AC adapter
Communication processor	P1010E cores running at 1000 MHz
Operating temperature	0 ^{o}C to 70 ^{o}C (room temperature)
Storage temperature	–25 ^{o}C to 85 ^{o}C
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	 6692 mil (170 mm) 6692 mil (170 mm) 62 mil

2.4 Mechanical Data

This figure shows the P1010RDB-PB dimensions. The board measures 170 mm × 170 mm (6693 mil × 6693 mil) integrated in a mini-ITX chassis.

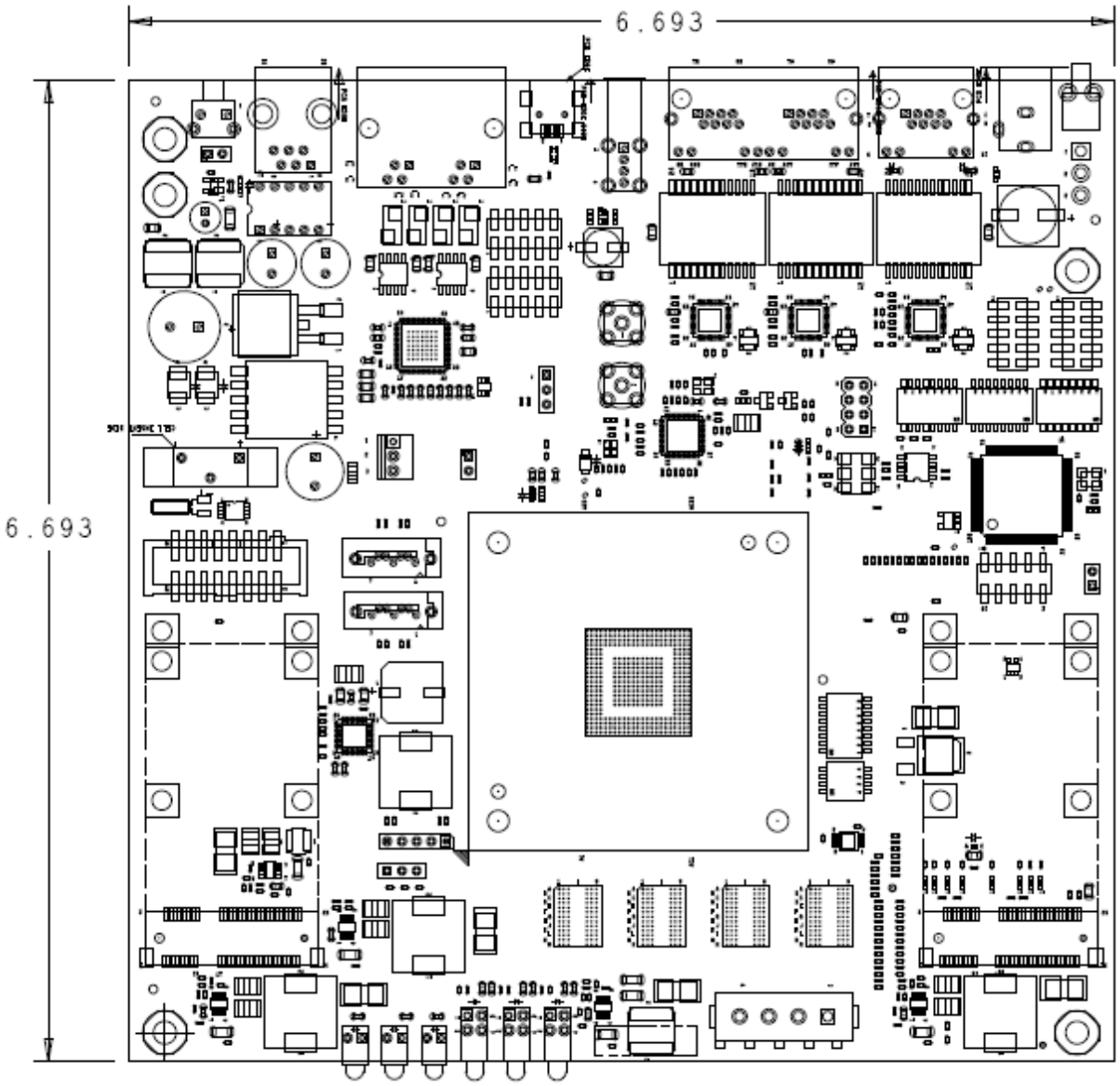

Figure 2-2. Dimensions of the RDB

Chapter 3
Hardware Description

3.1 Memory Interface

3.1.1 Description

The memory interface on the RDB is configured as DDR3 and is implemented as a single bank discrete chips (x8). ECC is not supported on the design. The memory size supported on the board is shown in the following table.

Table 3-1. Memory Size

P1010RDB-PB (32-bit)
1GB (4 chips * 2Gbit chips)/8bits

The PCB design is capable of running up to a clock rate of 400 MHz (800 MHz data rate).

The DDR3 interface uses the SSTL driver/receiver and 1.5 V power. A VREF1.5 V/2 is needed for all SSTL receivers in the DDR3 interface. For details on DDR3 timing design and termination, refer to the Freescale application note AN2582 (Hardware and Layout Design Considerations for DDR Memory Interfaces).

Signal integrity test results show this design does not require terminating resistors (series resistor (RS) and termination resistor (RT)) for the discrete DDR3 devices used. DDR3 supports on-die termination; the DDR3 chips and P1010E are connected directly. The interface is 1.5 V and is provided by an on-board voltage regulator. VREF, which is half the interface voltage, or 0.75 V, is supplied by the same voltage regulator.

This figure shows the DDR3 SDRAM controller connection.

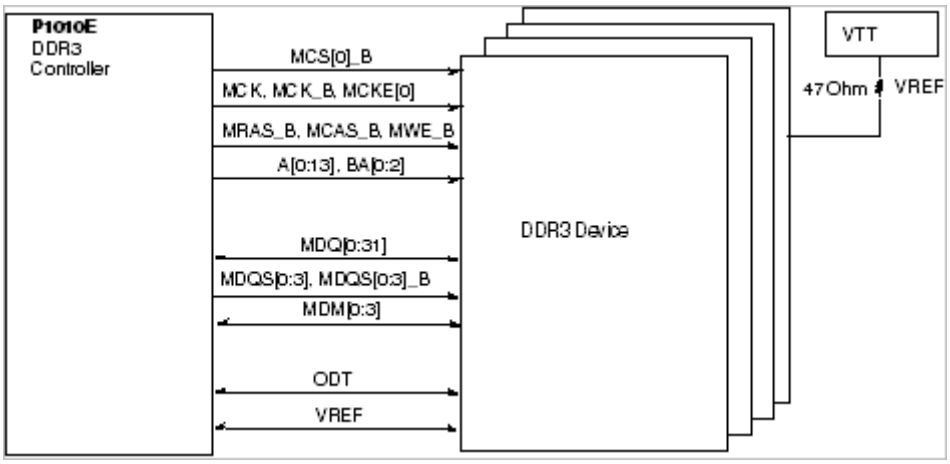

Figure 3-1. DDR3 SDRAM Connection

3.1.2 Termination

The DDR3 address, control, and command signals are terminated to the VTT rail via a 47 Ohm resistor.

3.2 SerDes Interfaces (PCIe/SGMII/SATA)

3.2.1 Description

P1010E supports the SGMII, SATA and PCI Express high-speed I/O interface standards. The following two tables detail SerDes1 and SerDes2 connections respectively.

Table 3-2. SerDes1 Connectivity

SerDes1 Lane	Mode	Connected to	Comment
Lane 0	PCI Express 1	Mini-PCIe slot	Used for 802.11b/g/n or 802.11ac WLAN type cards
Lane 1	PCI Express 2	Mini-PCIe slot	Used for 802.11b/g/n or 802.11ac WLAN type cards
Lane 2	SGMII2	SGMII PHY	—
Lane 3	SGMII3	SGMII PHY	—

Table 3-3. SerDes2 Connectivity

SerDes2 Lane	Mode	Connected to	Comment
Lane 0	SATA0	internal SATA Slot	—
Lane 1	SATA1	internal SATA Slot	—

3.2.2 PCIe

On the RDB, lanes 0 and 1 are configured as two independent x1 PCI Express Interfaces. These interfaces are compliant with the PCI Express Base Specification Revision 1.1. The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane. Support Root Complex (RC) and EndPoint (EP) configurations.

3.2.3 SATA

On the P1010RDB-PB, Serdes2 are configured as two independent SATA 2.0 Controllers. It can support two SATA hard drive on board. But default no supply hard drive in the kit.

3.2.4 SGMII

On the P1010RDB-PB, lane 2 and lane 3 of Serdes1 are used in SGMII mode. The serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signalling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse.

3.2.5 SerDes Clocking

The clocking for the SerDes interface is 100MHz provided by the IDT clock chip.

3.3 Integrated Flash Controller (IFC) Interface

The integrated flash controller (IFC) is used to access the external NAND Flash, NOR Flash and CPLD. To interface with the standard memory device, an address latch is needed on the upper address bits since they are multiplexed with the data bus. The IFC_AVD is used as the latching signal. The followings modules are connected to the IFC:

- 32 Mbyte NOR flash memory
- 2 Gbyte NAND flash memory
- CPLD (Lattice LCMXO256C)

3.3.1 NOR Flash Memory

P1010RDB-PB provides a 32Mbyte of NOR flash memory. The flash memory used is configured in a 16-bit port size. This figure shows the hardware connections for the flash memory.

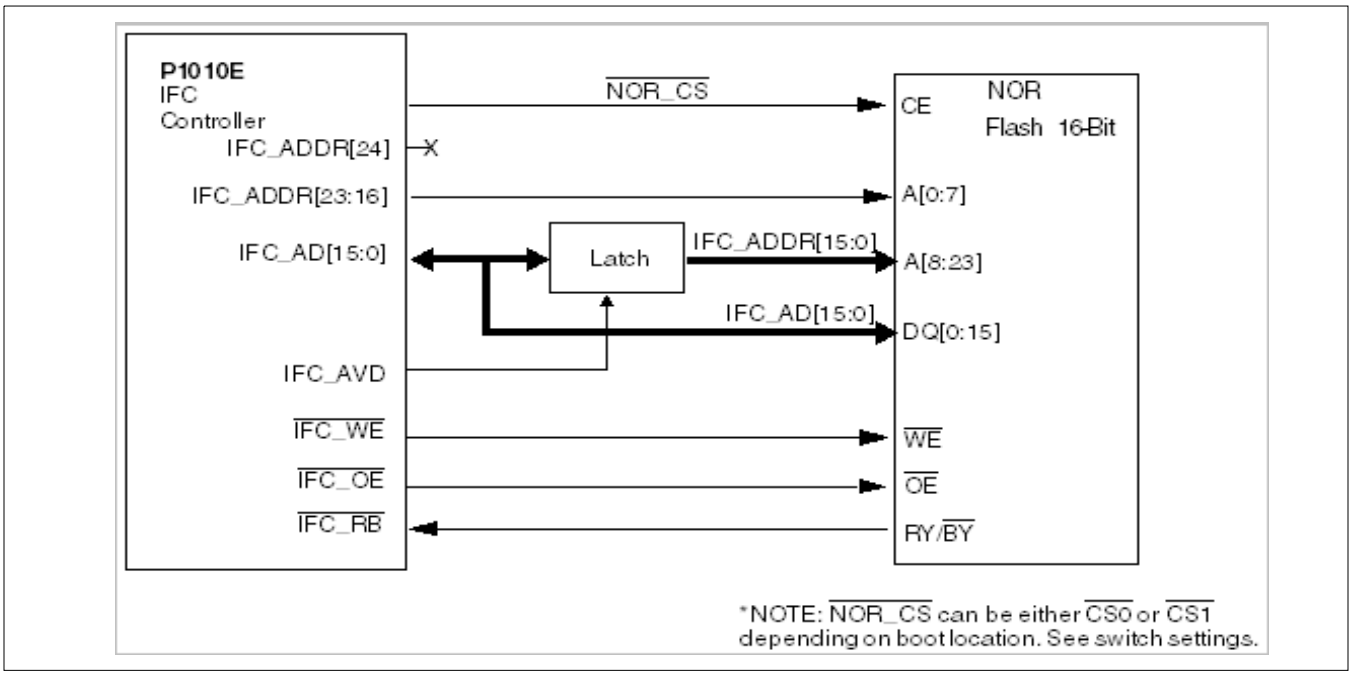

Figure 3-2. NOR Flash Connection

3.3.2 NAND Flash Memory

The P1010E has native support for NAND Flash memory through its NAND Flash control machine (FCM). The P1010RDB-PB implements an 8-bit, 4K page-size SLC NAND Flash with 2 Gbyte capacity. This figure shows the NAND Flash connection.

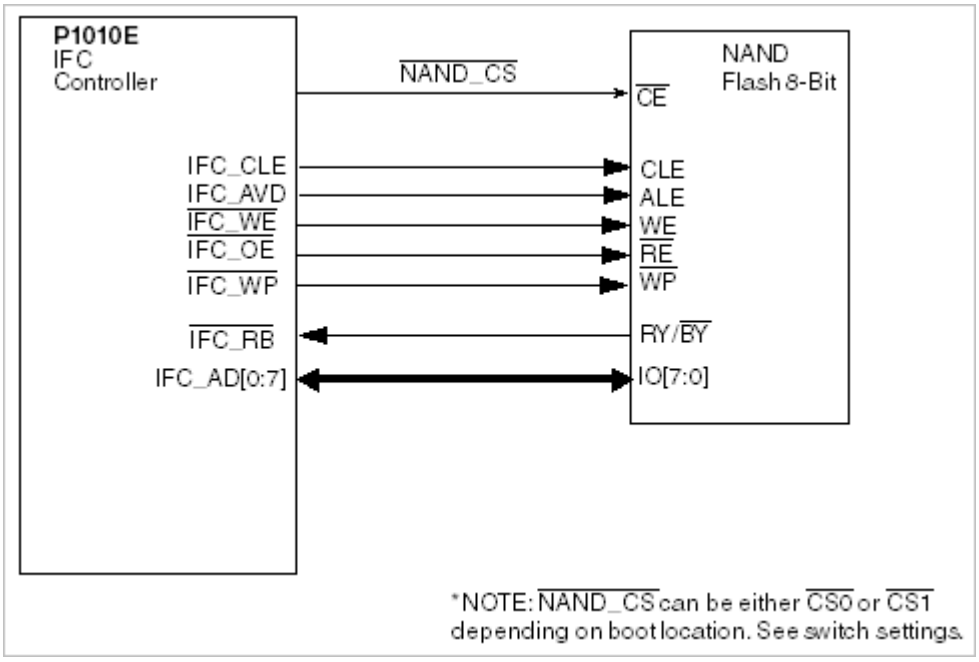

Figure 3-3. NAND Flash Connection

3.3.3 Lattice CPLD

Lattice CPLD LCMXO256C is connected to the P1010 IFC on P1010RDB-PB. This gives the processor the ability to access the 8-bit registers in the CPLD via GPCM. Refer Section "CPLD Specification" for more details.

This figure shows the connection between CPLD and the P1010E IFC controller.

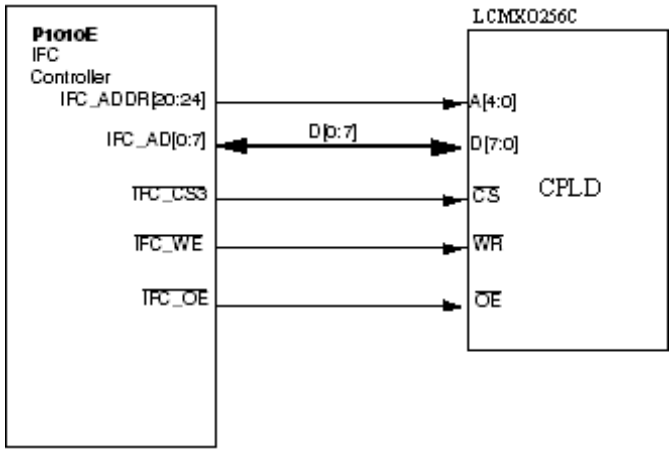

Figure 3-4. CPLD Connection

This table summarizes the IFC connectivity.

Table 3-4. IFC Connectivity

IFC chip select	Manufacturer	Device	Comment
IFC_CS0 or IFC_CS1 Assignment dependent on SW3[4]	Spansion	S29GL256S90TFI010	NOR FLASH memory 32 Mbyte (16bit)
IFC_CS0 or IFC_CS1 Assignment dependent on SW3[4]	Micron	MT29F16G08ABACAWP	NAND Flash 2 Gbytes (8bit)
IFC_CS2	—	—	—
IFC_CS3	Lattice	LCMXO256C	CPLD

3.4 Ethernet

The RDB supports a total of three ethernet ports.

3.4.1 eTSEC1 10/100/1000 BaseT Interface

eTESC1 is set to operate in RGMII mode. It connects to a Qualcomm Atheros RGMII PHY (AR8033), as shown in the following figure.

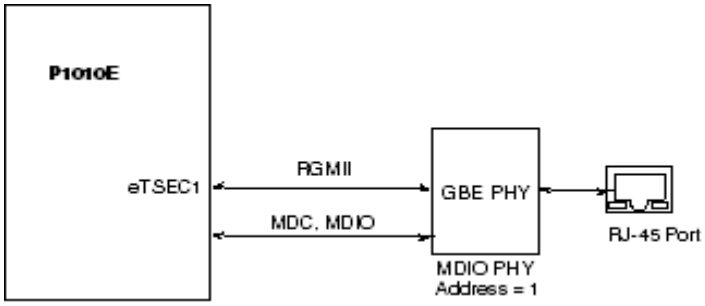

Figure 3-5. RGMII Interface Connection

3.4.2 eTSEC2 10/100/1000 BaseT Interface

eTSEC2 is set to operate in SGMII and is directly connected to the Qualcomm Atheros SGMII PHY (AR8033), as shown in this figure.

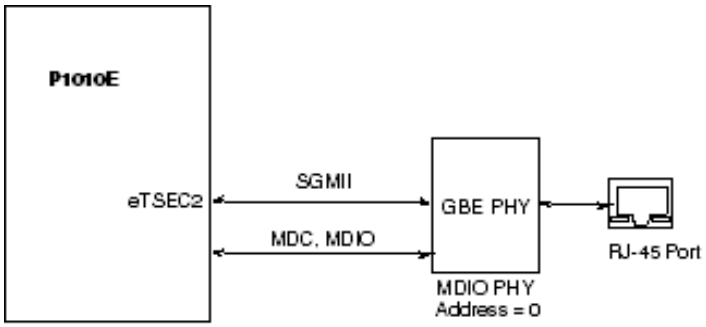

Figure 3-6. eTSEC2 Connection

3.4.3 eTSEC3 10/100/1000 BaseT Interface

eTSEC3 is set to operate in SGMII and is directly connected to the Qualcomm Atheros SGMII PHY (AR8033), as shown in this figure.

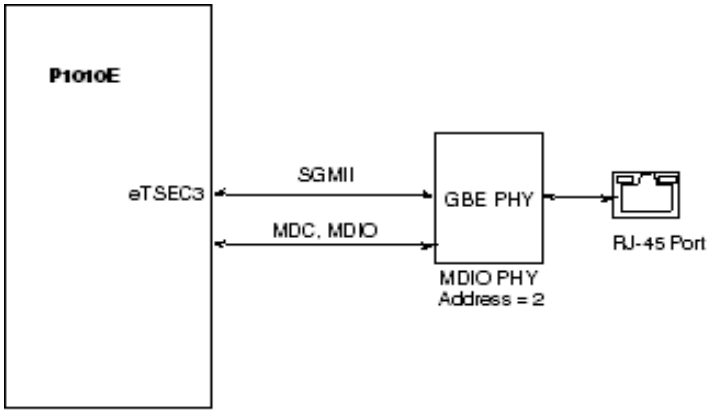

Figure 3-7. eTSEC3 Connection

3.4.4 Ethernet Management

This table details how the MDC and MDIO connections are made on the RDB.

Table 3-5. MDC/MDIO Connectivity

Device	PHY Address(Bin)
RGMII- AR8033	00001
SGMII2-AR8033	00000
SGMII3-AR8033	00010

3.4.5 Ethernet Ports

This figure shows how the ethernet ports are connected on the backside of the RDB chassis.

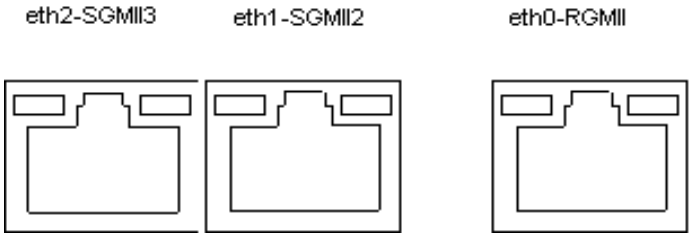

Figure 3-8. Ethernet Port Connectivity

3.5 eSPI

The eSPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The P1010E has the ability to boot from a SPI serial flash device in addition to supporting other peripheral devices conforming to the SPI standard.

On the RDB, a Spansion SPI flash memory is supported. In addition to it, the SPI interface is also connected to SLIC chip. SW3[2] will assign the eSPI chip selection (SPI_CS0_B) to SPI flash or SLIC chip. This table details the eSPI connections.

Table 3-6. eSPI Connectivity

eSPI Chip Select	Manufacturer	Part #	Comment
SPI_Flash_CS_N	Spansion	S25FL128S	16MB Spansion SPI Flash, (Default)
SPI_CS1_N	Zarlink	Le88266	SLIC/SLAC
SPI_CS_DAC_N	Microchip	MCP4921	12-bit DAC(Default: DNP)

3.6 eSDHC Interface

The enhanced SD host controller (eSDHC) provides an interface between host system and SD/MMC cards. The secure digital (SD) card is specifically designed to meet the security, capacity, performance, and,

environmental requirements inherent in emerging audio and video consumer electronic devices. Booting from eSDHC interface is supported via the processor's on-chip ROM.

On the RDB, a single connector is used for both SD and MMC memory cards as shown in this figure.

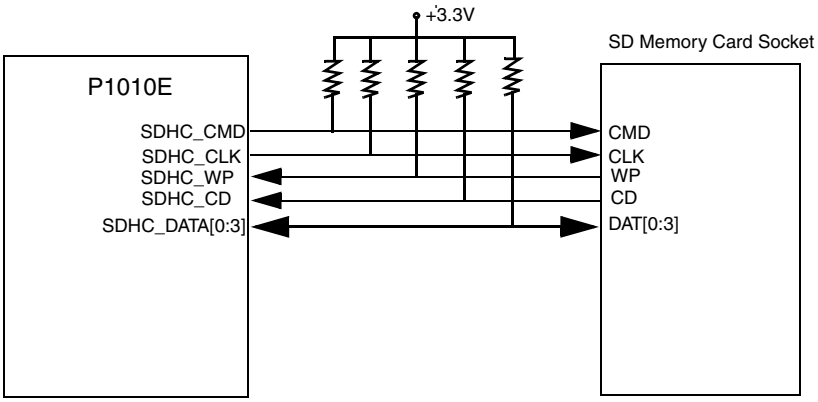

Figure 3-9. SD Memory Card Connection

The SDHC are multiplexed with IFC address lines signals. The selection between them is controlled by I2C device signals or switch SW3[3]. When this function is enabled, IFC bus is not available.

This table lists the IFC/SDHC multiplexed signals.

Table 3-7. IFC/USB/SDHC Multiplexed Signals

IFC Signals	Alternative SDHC Signal
IFC_ADDR24	—
IFC_ADDR23	SDHC_CD
IFC_ADDR22	SDHC_WP
IFC_ADDR21	SDHC_DATA3
IFC_ADDR20	SDHC_DATA2
IFC_ADDR19	SDHC_DATA1
IFC_ADDR18	SDHC_DATA0
IFC_ADDR17	SDHC_CMD
IFC_ADDR16	SDHC_CLK
IFC_PERR	—
IFC_CLK1/$\overline{\text{IFC\_CS3}}$	—
IFC_PAR0	—

On the RDB, two 4-bit mux/demux bus switch chips are used to assign the multiplexed signals to IFC or SDHC device, as shown in this figure.

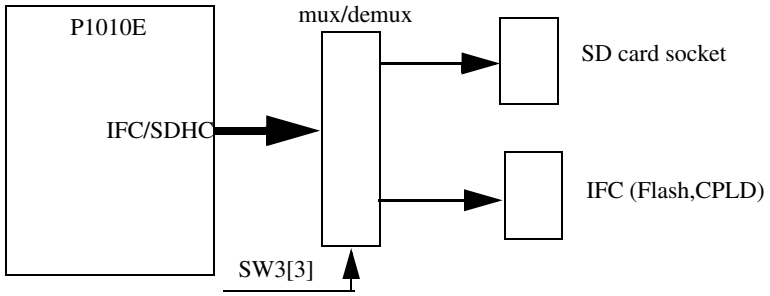

Figure 3-10. IFC/USB/SDHC Bus selection

3.7 GPIO

This table lists the GPIO pin usage on the RDB platform.

Table 3-8. GPIO Pin Usage

GPIO	Input / Output	Signal Name	Comment
GPIO00	input	USB_DRVVBUS	Used to drive USB power, not GPIO
GPIO01	input	USB_PWRFAULT	USB VBUS power fault, not GPIO
GPIO02	input	CKSTP_IN_N	Checkstop input, not GPIO
GPIO03	output	CKSTP_OUT_N	Checkstop output or therm IRQ, not GPIO
GPIO04	output	WLAN_LED1	GPIO04 output as miniPCIe1 LED indicator
GPIO05	output	WLAN_LED2	GPIO05 output as miniPCIe2 LED indicator
GPIO06	input/output	SPI_MOSI	eSPI MOSI, not GPIO
GPIO07	input/output	SPI_MISO	eSPI MISO, not GPIO
GPIO08	output	SPI_CLK	eSPI clock, not GPIO
GPIO09	output	SPI_CS0_N	eSPI chip selection, not GPIO
GPIO10	output	UARTCST1/TDM_TCLK	UART1 clear-to-send or TDM send clock, not GPIO
GPIO11	input	UART1_RTS_N	UART1 ready-to-send, not GPIO
GPIO12	input	TSEC1_RXD1	eTSEC1 receive data1, not GPIO
GPIO13	input	TSEC1_RX_CTL	eTSEC1 receive control line, not GPIO
GPIO14	input	TSEC1_RXCLK	eTSEC1 receive clock, not GPIO
GPIO15	input	TSEC1_GTX_CLK125	eTSEC1 transmit clock, not GPIO

3.8 Interrupts

This figure shows the external interrupts to the P1010E.

Note: Others IRQ are not used on board

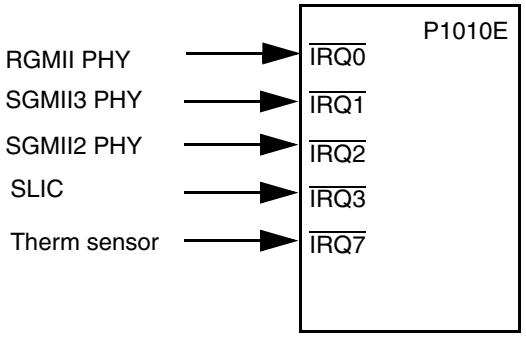

Figure 3-11. P1010E Interrupts

This table details how the interrupts are connected on the RDB platform.

Table 3-9. Interrupts

Name	Connection	Note
IRQ0	RGMII PHY AR8033	On-board Pull-up
IRQ1	SGMII3 PHY AR8033	On-board Pull-up
IRQ2	SGMII2 PHY AR8033	On-board Pull-up
IRQ3	TDM SLIC Le88266	On-board Pull-up
IRQ4	not used	On-board Pull-up
IRQ5	not used	On-board Pull-up
IRQ6	not used	On-board Pull-up
IRQ7	Therm sensor LM75BD	On-board Pull-up
IRQ8	not used	On-board Pull-up
IRQ9	not used	On-board Pull-up
IRQ_OUT	not used	On-board Pull-up

3.9 I2C

The P1010E device has two I2C controllers. On the RDB, the I2C buses are connected as shown in this figure. The M24256 serial EEPROM can be used to store configuration registers' values and/or user program if the P1010E boot sequencer is enabled. For details about the boot sequencer mode, refer to the *QorIQ P1010E Integrated Processor Reference Manual.* By default, the boot sequencer is not used and the boot code and initialization for the board is loaded from the local bus flash memory.

The following table shows all I2C device and address information on P1010RDB-PB.

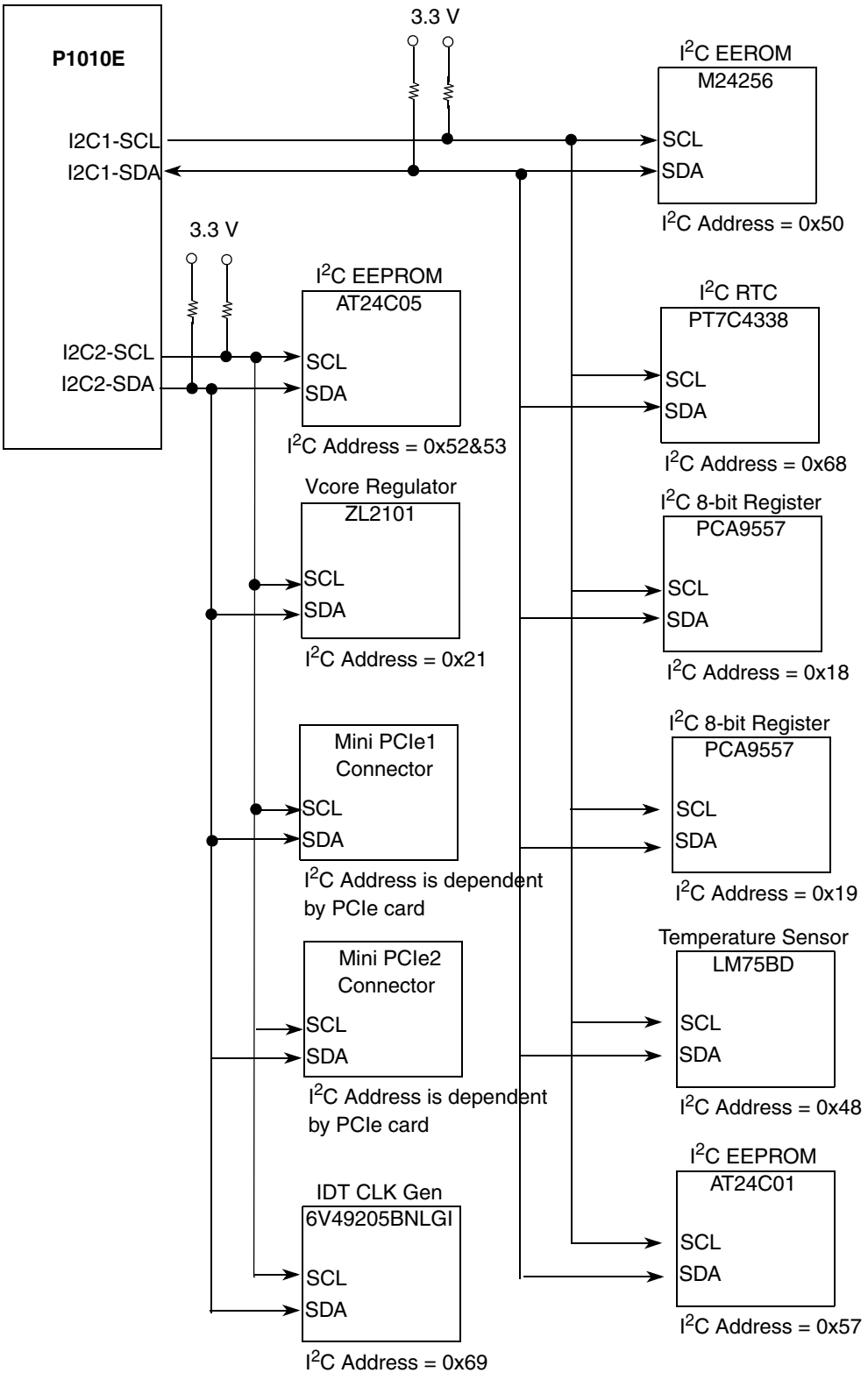

Figure 3-12. I2C Connection

Table 3-10. I^2C Bus Connections

I2C Bus	I2C Address	Manufacturer	Device	Comment
I2C1	50H	ST Microelectronics	M24256	Boot sequencer eeprom 256Kbits
I2C1	68H	Pericom	PT7C4338	Real time clock
I2C1	18H	NXP	PCA9557	8-bit I2C register
I2C1	19H	NXP	PCA9557	8-bit I2C register
I2C1	48H	NXP	LM75BD	Temperature Sensor
I2C1	57H	Atmel	AT24C01	System configuration EEPROM
I2C2	21H	Intersil	ZL2101	Vcore Regulator
I2C2	69H	IDT	6V49205BNLGI	Clock generator
I2C2	52H&53H	ON-Semiconductor	CAT24C05	Board SPD EEPROM
I2C2	—	—	Mini PCIe1 PCIe x1 Connector	I^2C Address is dependent by PCIe card
I2C2	—	—	Mini PCIe2 PCIe x1 Connector	I^2C Address is dependent by PCIe card

3.10 USB Interface

On P1010RDB-PB, USB interface is using the internal UTMI and is directly connected to a USB type A connector.

3.11 Dual RS-232 Ports

The P1010E device has two UART controllers. The RS-232 interface provides an RS-232 standard interconnection between the card and an external host. The serial connection is typically configured to run at 115.2 Kbps.

Each UART supports:

- Full-duplex operation.
- Software-programmable baud generators:
  - — Divide the input clock by 1 to (216 – 1)
  - — Generate a 16x clock for the transmitter and receiver engines
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions.
- Software-selectable serial interface data format that includes:
  - — Data length
  - — Parity
  - — 1/1.5/2 STOP bit

— Baud rate

- Overrun, parity, and framing error detection.

On RDB board, UART0 port is routed to a USB-to-RS232 chip and use for console port. UART1 port is routed to a 10 pin header.

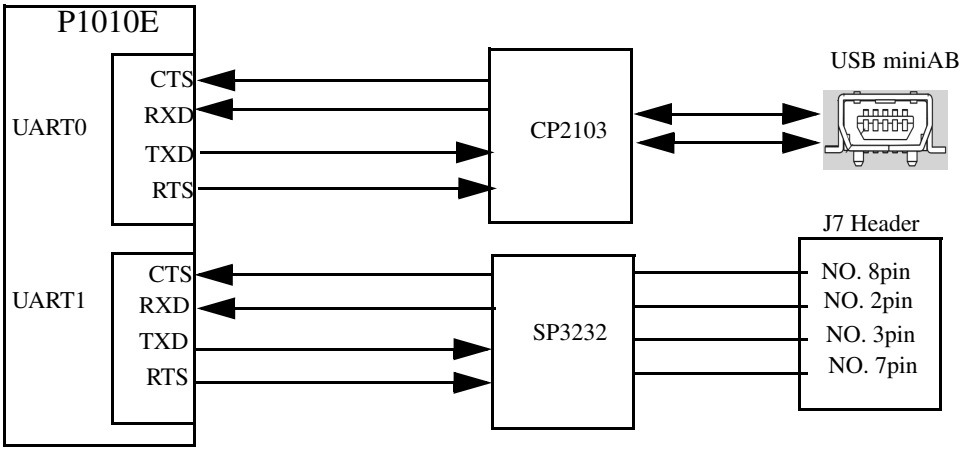

Figure 3-13. RS-232 Ports Connection

3.12 CAN

P1010E has dual Controller Area Network (CAN) controller (FlexCAN). P1010RDB-PB connects two CAN interfaces to two 10-pin header on board. In the kit, there are two cables which offered the connection from header to a standard female DB9 connector.

Each FlexCAN supports:

- Programmable bit rates upto 1Mbps
- Standard data and remote frames
- Extended data and remote frames
- Upto eight bytes data length
- Upto 64 message buffers (MB), each configurable as Rx or Tx
- Individual Rx mask registers per MB
- Rx FIFO with storage capacity of 6 frames and internal pointer handling
- Rx FIFO ID filtering
- Time stamp based on 16-bit free running timer

This table lists the pinout of the CAN DB9 connector.

Table 3-11. Pinout of the CAN DB9 Connector

DB9 Female Pin#	J9/J10 Header	Signal Description	Comments
1	1	N.A	Unused
2	2	CAN_L	Differential CAN negative signal
3	3	GND	Ground
4	4	N.A	Unused
5	5	GND	Ground
6	6	N.A	Unused
7	7	CAN_H	Differential CAN positive signal
8, 9, 10	8, 9, 10	N.A	Unused

TI SN65HVD230 CAN transceiver is applied in our RDB board. The transceiver is attached to the differential bus lines at pin CAN_H and CAN_L. Typically, the bus is a twisted pair of wires with a characteristic impedance of 120 ohm. On our P1010RDB-PB, there is a 120 ohm terminated resistor. If you connect to another CAN topology, it's helpful to minimize signal reflections on the bus.

3.13 Lattice CPLD

The Lattice CPLD is used for power up sequence control, POR setting control, system and peripherals reset etc. Refer Section "CPLD Specification" for more details.

3.14 POR Configuration

The POR configuration is based on switch setting and jumpers or resistors. When hard reset (HRESET) is asserted, the POR config begins to drive the POR config signals to the processor. The config signals remain asserted until the POR config signals have been properly latched by the processor.

3.15 JTAG/COP

The JTAG connection is provided by a direct connection to the appropriate header connector.

3.15.1 COP/JTAG Port

The common on-chip processor (COP) is part of the P1010E's JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, RS-232, and so on. A typical setup using a USB port emulator is shown in this figure.

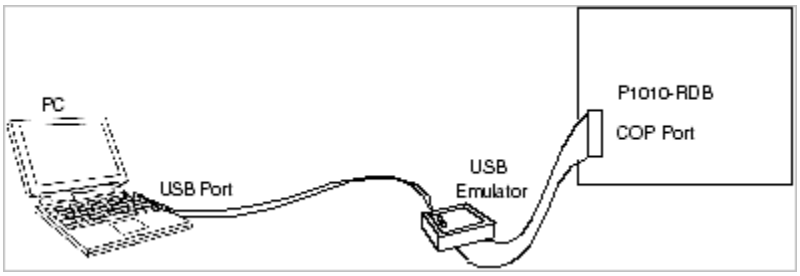

Figure 3-14. Connecting P1010RDB-PB to a USB Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in this figure.

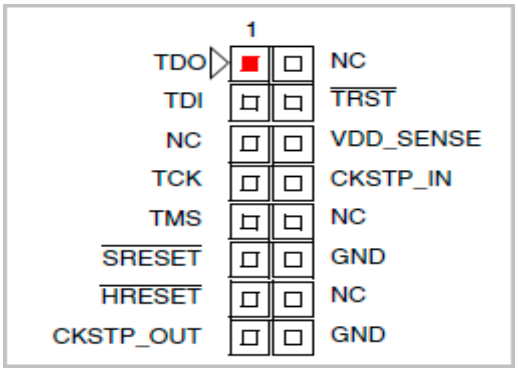

Figure 3-15. RDB COP Connector

This table details the connections made from the RDB COP connector.

Table 3-12. Connectivity from the COP Connector

Pin Number		
Pin #	Signal Name	Connection
1	TDO	Connected directly between the processor and JTAG/COP connector.
2	NC	Not connected
3	TDI	Connected directly between the processor and JTAG/COP connector.
4	TRST	Routed to the RESET PLD. TRST to the processor is generated from the PLD.
5	NC	Not connected
6	VDD_SENSE	Pulled to 3.3V via a 10 Ohm resistor
7	TCK	Connected directly between the processor and JTAG/COP connector.
8	CKSTP_IN	Connected directly between the processor and JTAG/COP connector.
9	TMS	Connected directly between the processor and JTAG/COP connector.
10	NC	Not connected
11	SRESET	Routed to the RESET PLD. SRESET to the processor is generated from the PLD.

Table 3-12. Connectivity from the COP Connector

Pin Number		
12	GND	Connected to ground
13	HRESET	Routed to the RESET PLD. HRESET to the processor is generated from the PLD.
14	KEY	Not connected
15	CKSTP_OUT	Connected directly between the processor and JTAG/COP connector.
16	GND	Connected to ground

3.16 DMA

The DMA function itself is not utilized on the RDB platform. Unused input pins are pulled high. Since certain DMA pins have POR functionality, these pins are connected on the platform.

3.17 Connectors, Headers, Push Buttons and LEDs

This table details the various headers on the RDB platform.

Table 3-13. Headers

Reference Designators	Used for	Mounted	Unmounted
J5	Remote reset header		Default.
J9	CAN1 Header	connect CAN1 signals to DB9 connector through a cable	Default, dis-connects CAN1 signals to DB9 connector through a cable
J10	CAN2 Header	connect CAN2 signals to DB9 connector through a cable	Default, dis-connects CAN2 signals to DB9 connector through a cable
J12	POVDD Header	Default: 1-2. Dis-connect fuse supply on POVDD	2-3, connect fuse supply on POVDD
J13	1588 Header	Used for 1588 port (DNP)	
J14	Chassis Fan power Header	Connect to chassis fan	dis-connect to chassis fan
J15	Program Jumper	COP connector program CPLD	Default, CPLD connector program CPLD
J17	COP/JTAG	Used for powerPC JTAG	
J18	CPLD Header	Used for programming the Lattice CPLD devices	
J19	HRST REQ	Default, Connects HRST_REQ(P1010 reset signal) to HRSTREQ_N (connected to CPLD)	Dis-connects HRST_REQ(P1010 reset signal) to HRSTREQ_N (connected to CPLD)
J22	GVDD Power select	Default, 2-3, GVDD=1.5V	1-2, GVDD=1.35V

3.18 Connectors

This table details all the connectors on the RDB platform.

Table 3-14. Connectors

Reference Designators	Used for	Note
J1	UART Port	UART0, miniUSB connector
J2	Power Input	Board power source
J3	Dual Ethernet Port	Right: SGMII2, Left: SGMII3
J4	TDM Port	1 TDM FXO port
J8	USBPHY CLK	For debug
J11	USB_ID	For debug
J16	SATA0	Internal SATA connector
J17	SATA1	Internal SATA connector
J23	SATA Power	power for SATA hard drive
J24	SD/MMC Card	SD/MMC card socket
U1	USB port	USB port
P1	Ethernet Port	RGMII port
P2	TDM Port	2 TDM FXS port
P3	MiniPCIE2	MiniPCIe 2 slot
P4	MiniPCIE1	MiniPCIe 1 slot

3.19 Battery Holder

The board contains an RTC that requires a battery in order to maintain the data inside the RTC. The battery holder (BT1) accommodates a CR-2032. This figure shows how to insert a battery.

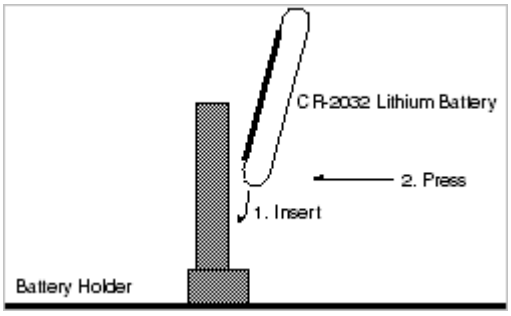

Figure 3-16. Installation of Battery

3.20 Push Button

This table details how the push button is used on the RDB platform.

Table 3-15. Push Buttons

Reference Designators	Used for
SW7	Reset

3.21 1588

The 1588 signals are routed to a 1588 header on the board (J13). The 1588 clock input into the processor can be controlled over the SPI interface through a 12-bit digital-to-analog converter (U14). The output of the DAC feeds directly into a precision VCXO which in turn is used to drive the 1588 clock into the processor. The DAC and VCXO combination allows the 1588 clock to be varied as needed for testing. These parts of this feature are not populated on board.

3.22 SLIC/SLAC and TDM Interface

The SLIC/SLAC and TDM interface is only applicable for P1010RDB-PB. The P1010E's TDM interface is connected to one dual SLIC/SLAC devices from Zarlink. The Zarlink Le88266 Automatic Battery Switching (ABS) VoicePort™ device implements a dual-channel telephone line interface by providing all the necessary voice interface functions from the high voltage subscriber line to the P1010E's digital TDM interface.

The Zarlink device provides a highly functional line interface which meets the requirements of short and medium loop (up to 1500 Ohms total at 1 REN) applications. Features include: high voltage switching regulator, line test capabilities, integrated ringing (up to 92-Vpk), worldwide software programmability with wideband capability, flexible signal generator with tone cadencing and caller ID generation. These device features allow for Voice over Broadband solutions to be enabled on the P1010RDB-PB.

Chapter 4
Power Related

4.1 DC Power Supply

A +12V@5A DC power supply for the RDB board. The rated power is 60W.

4.2 CPU_VDD

The CPU core voltage CPU_VDD rail is sourced from an Intersil switching regulator. The device used on the RDB is the ZL2101. CPU_VDD=1.0V

4.3 AVDD Signals

All AVDD pins are sourced by the CPU_VDD rail through the recommended filter circuit.

4.4 DDR

The memory interface power rails (VTT, GVDD, and VREF) are sourced by an MPS switching regulator MP1496 and an MPS memory termination regulator MP2007. For DDR3, GVDD=1.5V, VTT=0.75V and VREF = 0.75V.

4.5 SerDes

The SerDes rails (SVDD, XVDD) are sourced from the on-board CPU_VDD core voltage rail.

4.6 USB, SPI, eSDHC (CVDD)

Each of these rails are sourced directly from 3.3V rail, which is a dedicated power plane on the board.

4.7 Local Bus (BVDD)

This rail is sourced from 3.3V, which is a dedicated power plane on the board.

4.8 DUARTs, System Control, I2C, JTAG (OVDD)

This rail is sourced from 3.3V, which is a dedicated power plane on the board.

4.9 eTSECs (LVDD)

The LVDD rail is used for the TSEC I/Os and is configured for 2.5V operation. The rail is sourced from a 800mA LDO.

4.10 Mini-PCIe (+1.5V)

The +1.5V rail is used by the mini-PCIe slot and is sourced by a MPS switching regulator. The part used is the MP1496 device.

4.11 Mini-PCIe slot (+3.3V)

The +3.3V rail is used by the mini-PCIe slot and is sourced by a MPS switching regulator. The part used is the MP1497 device. It can supply 3A current.

4.12 Voltage Selection

The P1010E device supports multiple supply voltages on its I/O supplies. This table shows how the voltage selection pins are configured on the RDB platform.

Table 4-1. I/O Supply Voltage Selection

Signal Name	Connection	Comment
LVDD_SEL	Pulled high. LVDD = 2.5V	eTSEC1, 2, 3, Ethernet management, 1588
BVDD_VSEL[0:1]	Pulled high. BVDD = 3.3V	Local Bus, GPIO[8:15]
CVDD_VSEL[0:1]	Pulled high. CVDD = 3.3V	USB, SD/MMC, SPI

4.13 Clocking

An integrated IDT clock generator(6V49205B) supply the all clocks on board.

- A single-end 66.66 MHz clock source for the processor SYSCLK.
- A single-end 125 MHz clock source for TSEC1_GTX_CLK125.
- Three single-end 25 MHz clock source for Gigabit PHY chips.
- Two single-end 2.048 MHz clock source for TDM.
- A single-end 66.66 MHz clock source for CPLD.
- Four group differential 100MHz clock for all PCIe ports and SATA ports

4.14 Reset

All resets for the board are handled by the CPLD. Power-on reset is initiated by depressing the power switch if the card is in a chassis. Warm reset is initiated by pressing SW7 on the board. Software is also capable of initiating a warm reset by asserting the HRESET_REQ line from the processor.

Chapter 5
Switching

5.1 P1010RDB-PB Frequency and Boot Configuration (via Switches)

The RDB has user selectable switches for evaluating different frequency and boot options for the P1010E device. Table 5-1 and Table 5-2 describe the available options.

NOTE

All frequencies below assume that the input SYSCLK is set to 66.66 MHz for P1010RDB-PB.

Table 5-1. P1010RDB-PB Frequency Config Options

Switch SW1[4]	Switch SW1[5]	Switch SW1[6]	Switch SW1[7]	Switch SW5[1]	Switch SW5[5]	Switch SW5[6]	Switch SW5[7]	Switch SW5[8]	Switch SW2[2]	Platform (MHz)	Core Freq (MHz)	DDR Freq (MHz)
OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	400	800	800
ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	400	800	667
ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	333	667	667
ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	266	533	667
OFF	**ON**	**OFF**	**ON**	**ON**	**ON**	**OFF**	**ON**	**OFF**	**ON**	**400**	**1000**	**800**
ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	400	1000	667

Table 5-2. P1010RDB-PB Boot Rom Location Config Options

Switch Settings SW4[1]	Switch Settings SW4[2]	Switch Settings SW4[3]	Switch Settings SW4[4]	Value (Binary)	Meaning
OFF	ON	ON	OFF	0110	SPI
OFF	ON	ON	ON	0111	SDHC
ON	**OFF**	**ON**	**OFF**	**1010**	**8b NAND - 4K page size(default)**
ON	ON	ON	ON	1111	16b NOR

5.2 Multiplexed Bus Selection

P1010E IFC bus is multiplexed with SDHC and USB bus. Bus selection and IFC_CS0, 1 is decided by SW3[4] or I2C1 controller(PCA9557PW). SW3[4] can set the default setting and I2C1 can override the mode selection. This table details how the switch set the bus mode selection.

Table 5-3. P1010RDB-PB Bus Mode Selection Config Options

Switch Settings SW3[4]	Switch Settings SW3[3]	Meaning
X	OFF	IFC
X	ON	SDHC
OFF	X	CS0->NOR; CS1->NAND
ON	X	CS1->NOR; CS0->NAND

5.3 Read and Writing of Bus Selection Switch

There are two 8-bit I2C register allows software to override switch(SW3) and change frequency or boot location remotely without changing the physical switch. The I2C registers are implemented by Philips PCA9557 device. The register definition is shown in Table 5-4. The mapping between the I2C register bits and the switches are shown Table 5-5. The I2C switch is located on I2C2 and is accessible at address 18H.

Table 5-4. PCA9557 Register Definition

Name	Type	Function
Register 0	Read	Input port register
Register1	Read/Write	Output port register
Register 2	Read/Write	Input pins polarity inversion register =1, the corresponding port pin's polarity is inverted =0, the corresponding port pin's original polarity is retained Note that default value of this register is: Bit [7:4] = 1, polarity inverted Bit [3:0] = 0, polarity not inverted
Register 3	Read/Write	Configuration register =1, the corresponding port pin is enabled as an input =0, the corresponding port pin is enabled as an output Note that default value of this register is FF

Table 5-5. I2C register (U40) signal definition

I2C Register Bit	Comment
IO7	overrides SW3[2], and thereby controls SPI_SEL
IO6	PCB revision(PCBID1), read only
IO5	PCB revision(PCBID0), read only
IO4	overrides SW1[8], and thereby controls BANK_SEL
IO3	overrides SW3[4], and thereby controls BOOT_SEL
IO2	overrides SW3[3], and thereby controls BUS_SEL

Table 5-5. I2C register (U40) signal definition

I2C Register Bit	Comment
IO1	overrides SW3[1], and thereby controls CAN_TDM_SEL
IO0	reserved

Table 5-6. I2C register (U45) signal definition

I2C Register Bit	Comment
IO7	I2C1_GPIO[7:4]-CCB and Core frequency settings 1100- CCB=400MHz; Core-400MHz 1101- CCB=400MHz; Core=600MHz 1110- CCB=400MHz; Core=800MHz 1111- CCB=400MHz; Core=1000MHz 0100- CCB=333MHz; Core=500MHz 0101- CCB=333MHz; Core=667MHz 0110- CCB=333MHz; Core=833MHz 0111- CCB=333MHz; Core=1000MHz 1000- CCB=267MHz; Core=400MHz 1001- CCB=267MHz; Core=533MHz 1010- CCB=267MHz; Core=667MHz 1011- CCB=267MHz; Core=800MHz
IO6	
IO5	
IO4	
IO3	I2C1_GPIO3, DDR3 frequency selection: 0-667MHz; 1-800MHz
IO2	I2C1_GPIO[2:1] - boot location selection: 11-NOR; 10-NAND; 01:SPI; 00-SDHC
IO1	
IO0	I2C1_GPIO0, enable software control

5.4 Configuring Host/Agent Mode

This table shows how the 2 PCIe ports can be configured in either root complex or end point mode.

Table 5-7. P1010RDB-PB Host/Agent Config Options

Switch Settings SW5[3]	Switch Settings SW5[2]	Configuration	Meaning
X	ON	cfg_host_agt[1] = 1	P1010E as a root complex on PCIe2
X	OFF	cfg_host_agt[1] = 0	P1010E as a end point on PCIe2
ON	X	cfg_host_agt[0] = 1	P1010E as a root complex on PCIe1
OFF	X	cfg_host_agt[0] = 0	P1010E as a end point on PCIe1

5.5 Switches Configuration Options

This table lists all switches(SW1-5) configuration options that are available on the board.

Table 5-8. Switches Configuration Options

Switch	Signal Name	Signal Meaning	Setting
SW1[1]	CFG_IFC_PB2	Selects Nand flash corresponding pages per block	SW1[3:1] OFF OFF OFF : Reserved. SW1[3:1] OFF OFF ON : 2K pages per block SW1[3:1] OFF ON OFF : 1K pages per block SW1[3:1] OFF ON ON : 512 pages per block SW1[3:1] ON OFF OFF : 256 pages per block **SW1[3:1] ON OFF ON : 128 pages per block** SW1[3:1] ON ON OFF: 64 pages per block SW1[3:1] ON ON ON: 32 pages per block
SW1[2]	CFG_IFC_PB1		
SW1[3]	CFG_IFC_PB0		
SW1[4]	CFG_DDR_PLL1	DDR Clock PLL Ratio	SW1[5:4] OFF OFF: 8:1 SW1[5:4] OFF ON: 10:1 **SW1[5:4] ON OFF: 12:1** SW1[5:4] ON ON: Reserved
SW1[5]	CFG_DDR_PLL0		
SW1[6]	CFG_SYS_PLL2	CCB Clock PLL Ratio	SW5[8] SW1[7:6] OFF OFF OFF: 4:1 SW5[8] SW1[7:6] OFF OFF ON: 5:1 **SW5[8] SW1[7:6] OFF ON OFF: 6:1** SW5[8] SW1[7:6] others: Reserved
SW1[7]	CFG_SYS_PLL1		
SW1[8]	NOR_FBANKS	NOR Flash Bank	**OFF: Lower bank used for booting start, address 0xeff80000** ON: Upper bank used for booting start, address 0xeef80000
SW2[1]	HRST_REQ_N (cfg_sb_dis)	Secure boot configuration	OFF: P1010E is configured to be a trusted system **ON: P1010E is configured to be a non-trusted system**
SW2[2]	CFG_CORE0_PLL2	Core Frequence	see SW5[6-7].
SW2[3]	CAN1_TX/TDM_TX_DATA (cfg_boot_seq[1])	Boot sequencer configuration	ON OFF: Reserved OFF ON: Normal I2C addressing mode is used. ON ON: Extended I2C addressing mode is used. **OFF ON: Boot sequencer is disabled.**
SW2[4]	IFC_BCTL_S (cfg_boot_seq[0])		
SW2[5]	IFC_WE_B (cfg_ifc_flash_mode)	IFC Flash mode configuration	OFF:cfg_rom_loc selected for NOR Boot: Reserved; NAND Boot: Bad block indicator is at page 0 and last page of each block. **ON:cfg_rom_loc selected for NOR Boot: Normal async NOR Flash; NAND Boot: Bad block indicator is at page 0 and page 1 of each block.(Default)**
SW2[6]	CFG_IFC_ADM	IFC address shift mode configuration	OFF:Reserved. **ON: Higher order address bits are multiplexed with data on IFC_AD[0:15]**
SW2[7]	CFG_CPU_BOOT	CPU Boot configuration	**OFF: e500 core is allowed to boot without waiting for configuration by an external master.** ON:CPU boot hold off mode. The e500 core is prevented from booting until configured by an external master.
SW2[8]	CFG_SVR	Personality Selection	OFF: Reserved. **ON: Must be high during power on reset sequence**
SW3[1]	CAN_TDM_SEL	CAN/TDM Selection	OFF: CAN is selected. **ON: TDM is selected.**

Table 5-8. Switches Configuration Options (continued)

Switch	Signal Name	Signal Meaning	Setting
SW3[2]	SPI_SEL	SPI Flash/TDM selection	**OFF: SPI Flash is selected.** ON: TDM SPI is selected.
SW3[3]	BUS_SEL	IFC/SDHC bus selection	**OFF: IFC is selected.** ON: SDHC is selected.
SW3[4]	BOOT_SEL	IFC CS selection	OFF: NOR boot, CS0=NOR, CS1=NAND. **ON: NAND boot, CS0=NAND, CS1=NOR.**
SW3[5]	CFG_IFC_ECC0	IFC ECC Settings	**SW3[5:6] OFF OFF: ECC disable** SW3[5:6] ON OFF: 4b correction SW3[5:6] ON ON: 8b correction SW3[5:6] OFF ON: ECC disable
SW3[6]	CFG_IFC_ECC1		
SW3[7]	CLKGEN_FS0	SYSCLK frequency	**SW3[7:8] OFF OFF: 66.66MHz** SW3[7:8] ON OFF: 100MHz SW3[7:8] OFF ON: 80MHz SW3[7:8] ON ON: 83.33MHz
SW3[8]	CLKGEN_FS1		
SW4[1]	CFG_ROM_LOC0	Boot ROM location	SW4[1-4] OFF ON ON OFF: SPI Boot SW4[1-4] OFF ON ON ON: SDHC Boot **SW4[1-4] ON OFF ON OFF: NAND Boot** SW4[1-4] ON ON ON ON: NOR Boot See Table 5-2 for details
SW4[2]	CFG_ROM_LOC1		
SW4[3]	CFG_ROM_LOC2		
SW4[4]	CFG_ROM_LOC3		
SW5[1]	CFG_PLAT_SPEED	Platform speed	OFF: Platform clock frequency is less than 300 MHz. **ON: Platform clock frequency is equal to or greater than 300 MHz.**
SW5[2]	CFG_HOST_AGT1	PCIE host/agent configuration	OFF: Device acts as an endpoint on PCI Express 2 interface **ON: Device acts as a root complex on PCI Express 2 interface**
SW5[3]	CFG_HOST_AGT0		OFF: Device acts as an endpoint on PCI Express 1 interface **ON: Device acts as a root complex on PCI Express 1 interface**
SW5[4]	CFG_DRAM_TYPE	DDR type	OFF:1.35V DDR3 technology **ON: 1.5V DDR3 technology**
SW5[5]	CFG_CORE_SPEED	Core speed	OFF: Core clock frequency is less than 450 MHz. ON: Core clock frequency is greater than or equal to 450 MHz.
SW5[6]	CFG_CORE0_PLL1	e500 core PLL ratio	SW2[2] SW5[6:7] OFF ON OFF: 1:1 SW2[2] SW5[6:7] ON ON OFF: 1.5:1 SW2[2] SW5[6:7] OFF OFF ON: 2:1 **SW2[2] SW5[6:7] ON OFF ON: 2.5:1** SW2[2] SW5[6:7] OFF ON ON: 3:1 SW2[2] SW5[6:7] others: reserved
SW5[7]	CFG_CORE0_PLL0		
SW5[8]	CFG_SYS_PLL0	CCB Clock PLL Ratio	see SW1[6:7]

Chapter 6
CPLD Specification

6.1 Overview

This section describes the CPLD specification and user register interface in P1010RDB-PB.

6.2 CPLD Key Features

- Power on sequence control
  - Power on CPU VDD, GVDD
- P1010 Reset Signal Generation and Distribution

  The system reset will have following features:
  - Power on reset
  - CPU reset by HRESET_REQ_N
  - Manual reset
- These Reset signals generation:
  - CPU_HRST_N
  - DDR_RST_N;
  - FLSH_RST_N;
  - SLIC_RST_N;
  - SGMII2_RST_N;
  - SGMII3_RST_N;
  - RGMII_RST_N
- Revision Logic:
  - 8 bit CPLD Revision: 4 bit major version and 4 bit minor version
- POR control
  - DIP Switch control POR settings
  - I2C register control POR settings

6.3 CPLD Pin Definition

6.3.1 Reset Logic

Table 6-1. P1010RDB-PB CPLD Reset Logic Pins

Pin Name	In/Out	Description
RST_PLD_N	IN	Manual Reset; From MAX811
HRSTREQ_N	IN	HW Reset Req; From CPU
COP_HRST_N	IN	HW Reset; From JTAG
COP_TRST_N	IN	Test Reset; From JTAG
COP_SRST_N	IN	SW Reset; From JTAG
CPUHRST_SRC_N	OUT	HW Reset; To the CPU, SLIC, RMGII, SGMII, flash, PCIe
DDR_RST_N	OUT	DDR Reset; To DDR silicon

6.3.2 Logic Bus Logic

Table 6-2. P1010RDB-PB CPLD IFC Bus Logic Pins

Pin Name	In/Out	Description
IFC_WE_B	IN	Write enable; From CPU
IFC_OE_B	IN	Read enable; From CPU
IFC_CS3_N	IN	Chip select; From CPU
IFC_ADDR[20:24]	IN	Address bus; From CPU
CPLD_IFC_AD[0:15]	IN/OUT	Data Bus; From/To CPU

6.3.3 Power Control Logic

Table 6-3. P1010RDB-PB CPLD Power Control Logic Pins

Pin Name	In/Out	Description
PS_VCORE_PG	IN	CPU core voltage power good; From ZL2101
CTL_VCORE_EN	OUT	CPU core voltage enable; To ZL2101
GVDD_PWR_ON	OUT	DDR voltage power enable; To DDR power supply
CTL_VCORE_MGN	OUT	CPU core voltage margin enable; To ZL2101

6.3.4 Others Logic

Table 6-4. P1010RDB-PB CPLD Others Logic Pins

Pin Name	In/Out	Description
PLD_CLK	IN	32.768KHz clock. Used to count the cycle time for the reset time
HIGH_CLK_CPLD	IN	66.66MHz clock input. Used to control POR reset timing.
I2C1_GPIO[0:7]	IN	I2C GPIO input
CFG_DRAM_TYPE	IN	DIP switch setting input for cfg_dram_type POR
CFG_CORE0_PLL[0:2]	IN	DIP switch setting input for cfg_core0_pll[0:2] POR
CFG_IFC_ADM	IN	DIP switch setting input for cfg_ifc_adm POR
CFG_IFC_PB[0:2]	IN	DIP switch setting input for cfg_core0_pll[0:2] POR
CFG_DDR_PLL[0:1]	IN	DIP switch setting input for cfg_ddr_pll[0:1] POR
CFG_SYS_PLL[0:2]	IN	DIP switch setting input for cfg_sys_pll[0:2] POR
CFG_PLAT_SPEED	IN	DIP switch setting input for cfg_plat_speed POR
CFG_HOST_AGT[0:1]	IN	DIP switch setting input for cfg_host_agt[0:1] POR
CFG_CORE_SPEED	IN	DIP switch setting input for cfg_core_speed POR
IFC_AVD	OUT	Output for POR cfg_dram_type
IFC_PAR1	OUT	Output for POR cfg_plat_speed
IFC_CLE	OUT	Output for POR cfg_host_agt[0]
CLK_EN	OUT	Output to enable clock generator
CLKGEN_REF	OUT	Output to select PCIe reference clock frequency

6.3.5 CPLD Register Map

6.3.5.1 Memory Map

CPLD registers are memory mapped to P1010 via IFC and supposed to be accessed as SRAM. This table lists the peripherals' data bus width and memory map.

Table 6-5. P1010RDB-PB CPLD Memory Map

Address	CS	Bank size	Device	Data width	Access
0xFFB00000-0xFFB0001F	CS3	32byte	CPLD	8bit	Read

6.3.5.2 Register Map

This table defines CPLD registers.

Table 6-6. P1010RDB-PB CPLD Register Map

Base Address	Addr Offset	Access type	Description	Register Name	Defaul t Value
0xFFB00000	0	R	Bit[3:0]: CPLD minor version register Bit[7:4]: CPLD major version register	cpld_ver	0x10
	0x1	R	Bit[3:0]: reserved Bit[7:4]: boot location register	boot_location[3:0]	0x05

6.3.5.3 Software control POR setting u-boot commands

- SDK u-boot for P1010RDB-PB has integrated the I2C command to change boot location.
  - => run boot_bank0 //board boot from NOR bank0
  - => run boot_bank1 //board boot from NOR bank1
  - => run boot_nand //board boot from NAND flash
  - => run boot_sd //board boot from sd card
  - => run boot_spi //board boot from SPI flash
- SDK u-boot for P1010RDB-PB has integrated the I2C command to control bus.
  - => mux ifc //board IFC bus is enabled, SDHC bus is disabled.
  - => mux sdhc //board SDHC bus is enabled, IFC bus is disabled.

Appendix A
Revision History

This appendix provides a list of the major differences between current *P1010RDB-PB user guide* and its previous revisions.

A.1 Version Number 0

This is the initial version of the P1010RDB-PB User Guide.