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FRDMDUALK3664EVB evaluation board

Rev. 1 — 6 September 2022   **User manual**

Document information

Information	Content
Keywords	BMS, TPL, S32K344
Abstract	This document is the user manual for dual MC33664 evaluation board.

Revision history

Rev	Date	Description
1	20220906	initial version

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2   FRDMDUALK3664EVB
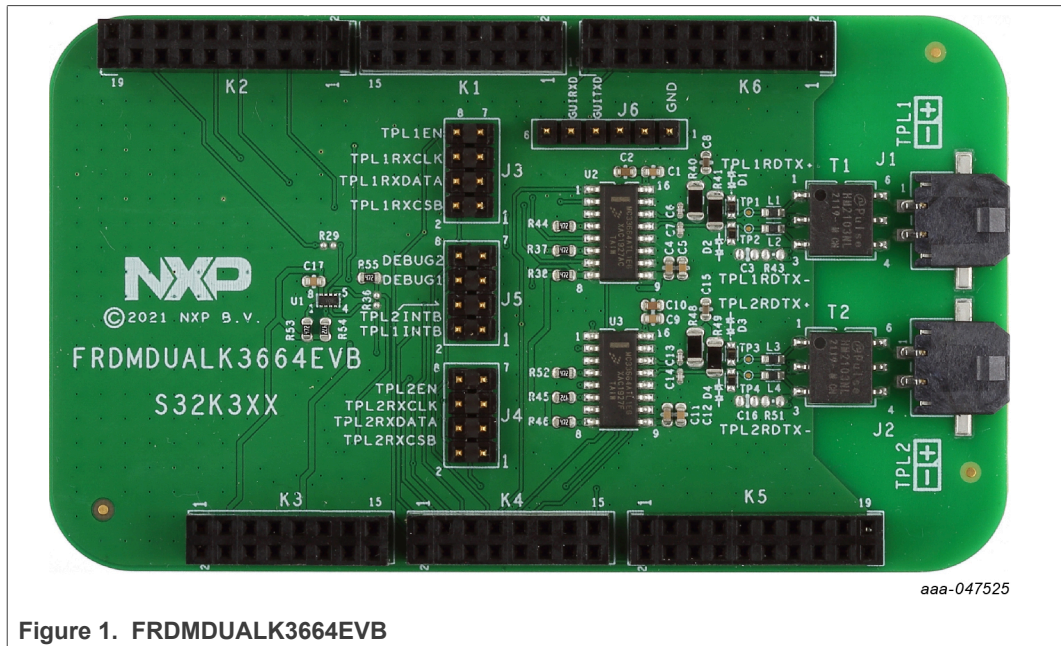
Figure 1. FRDMDUALK3664EVB

3   Introduction

This document is the user manual for the FRDMDUALK3664EVB evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of MC33664, isolated network high-speed transceiver.

The scope of this document is to provide the user with information to evaluate the MC33664, isolated network high-speed transceiver. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

Table 1. MC33664 evaluation board (EVB) options

	FRDMDUALK3664EVB	FRDMDUAL33664EVB	FRDM33664EVB
Link	http://www.nxp.com/FRDMDUALK3664EVB	http://www.nxp.com/FRDMDUAL33664EVB	http://www.nxp.com/FRDM33664BEVB
Intended microcontroller	S32K3x4EVB-Q172	S32K144EVB-Q100	FRDMKL25Z
Link	http://www.nxp.com/part/S32K3X4EVB-Q172	http://www.nxp.com/part/S32K144EVB-Q100	http://www.nxp.com/FRDM-KL25Z
MC33664	dual	dual	single
VIO options	3.3 V 5 V	3.3 V 5 V	3.3 V 5 V
Fault line support	no	no	yes

4   Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported devices on http://www.nxp.com.

The information page for FRDMDUALK3664EVB is at http://www.nxp.com/FRDMDUALK3664EVB. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick reference information applicable to using the FRDMDUALK3664EVB, including the downloadable assets referenced in this document.

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5   Getting ready

Working with the FRDMDUALK3664EVB requires the kit contents, additional hardware, and software, depending on the use case.

5.1   Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 50 cm transformer physical layer (TPL) bus cable
- Quick start guide

5.2   Additional hardware

- Use with the S32K3x4EVB-Q172 (recommended)
- Use with other microcontroller platform (requires breadboard design)
- Use as standalone EVB, requires 5.0 V, 200 mA power supply (optional 3.3 V power supply 200 mA), and signal stimulation with signal generator

6   Getting to know the hardware

6.1   Kit overview

The FRDMDUALK3664EVB is a hardware tool for evaluation and development and is ideal for rapid prototyping of an isolated network high-speed transceiver. It can be used to evaluate the features of the MC33664A device.

The evaluation board allows the user to connect serial peripheral interface (SPI) signals from the MCU to the device and be able to create bit pulses transmission to the bus through the transformer. The messages received by the device can be converted bit by bit and transferred to the MCU by SPI.

6.1.1   FRDMDUALK3664EVB features

- Two MC33664ATL1EG isolated communication transceivers in a SO16 package
- Isolated communication by transformers with connector
- Single TPL chain interface (requires two SPIs)
- Dual TPL chain interface (requires three SPIs)
- Compatible to S32K3x4EVB-Q172
- Connector for FTDI USB-to-serial cable (TTL-232R-5V)

Note: *The FRDMDUALK3664EVB does not support the fault line feature.*

6.2   Kit featured components

Figure 2 identifies important components on the board and Table 2 provides additional details on these components.

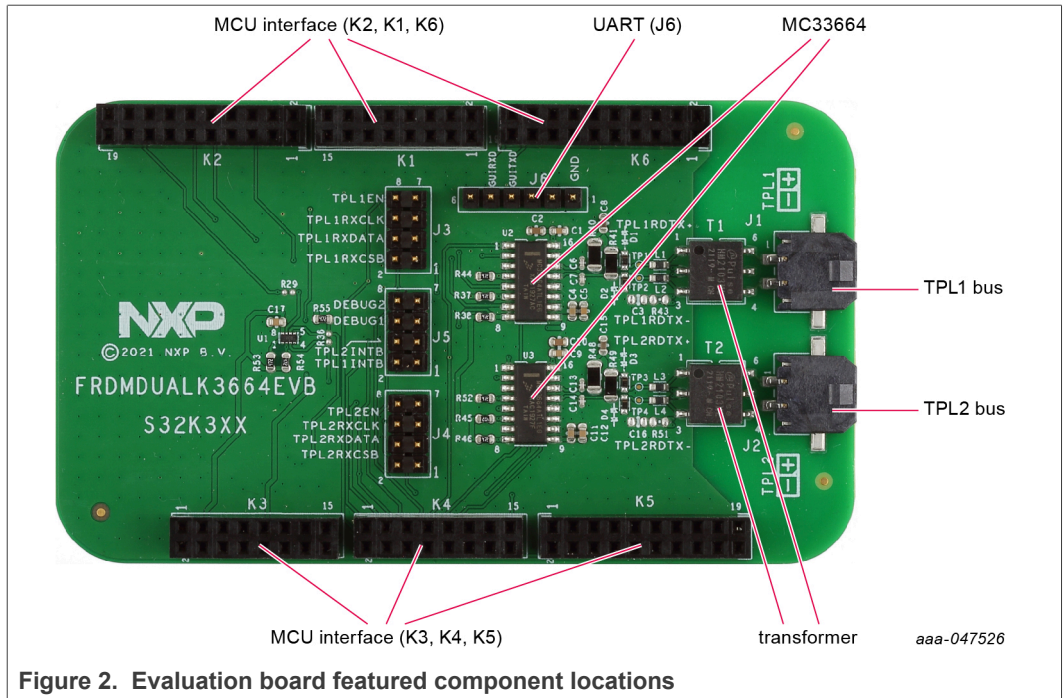**Figure 2. Evaluation board featured component locations**

Table 2. Evaluation board component descriptions

Name	Description
MCU interface (K2, K1, K6)	interface pin for microcontroller development platform (recommended S32K3x4EVB-Q172)
UART (J6)	universal asynchronous receiver transmitter (UART) connection (for example, for FTDI cable)
MC33664	isolated network high-speed transceiver
Transformer	bus isolator transformer (T1, T2)
TPL1 bus	TPL1 bus interface
TPL2 bus	TPL2 bus interface
MCU interface (K3, K4, K5)	interface pin for microcontroller development platform (recommended S32K3x4EVB-Q172)

6.2.1 MC33664: Isolated network high-speed transceiver

6.2.1.1 General description

The MC33664 is a SMARTMOS transceiver physical layer transformer driver designed to interface a microcontroller conveniently to a high speed isolated communication network. MCU SPI data bits are directly converted to pulse bit information and transferred to the bus network.

Slave response messages use the same structure to send pulse bit information to the MC33664, which is converted and sent back to the MCU as an SPI bit stream.

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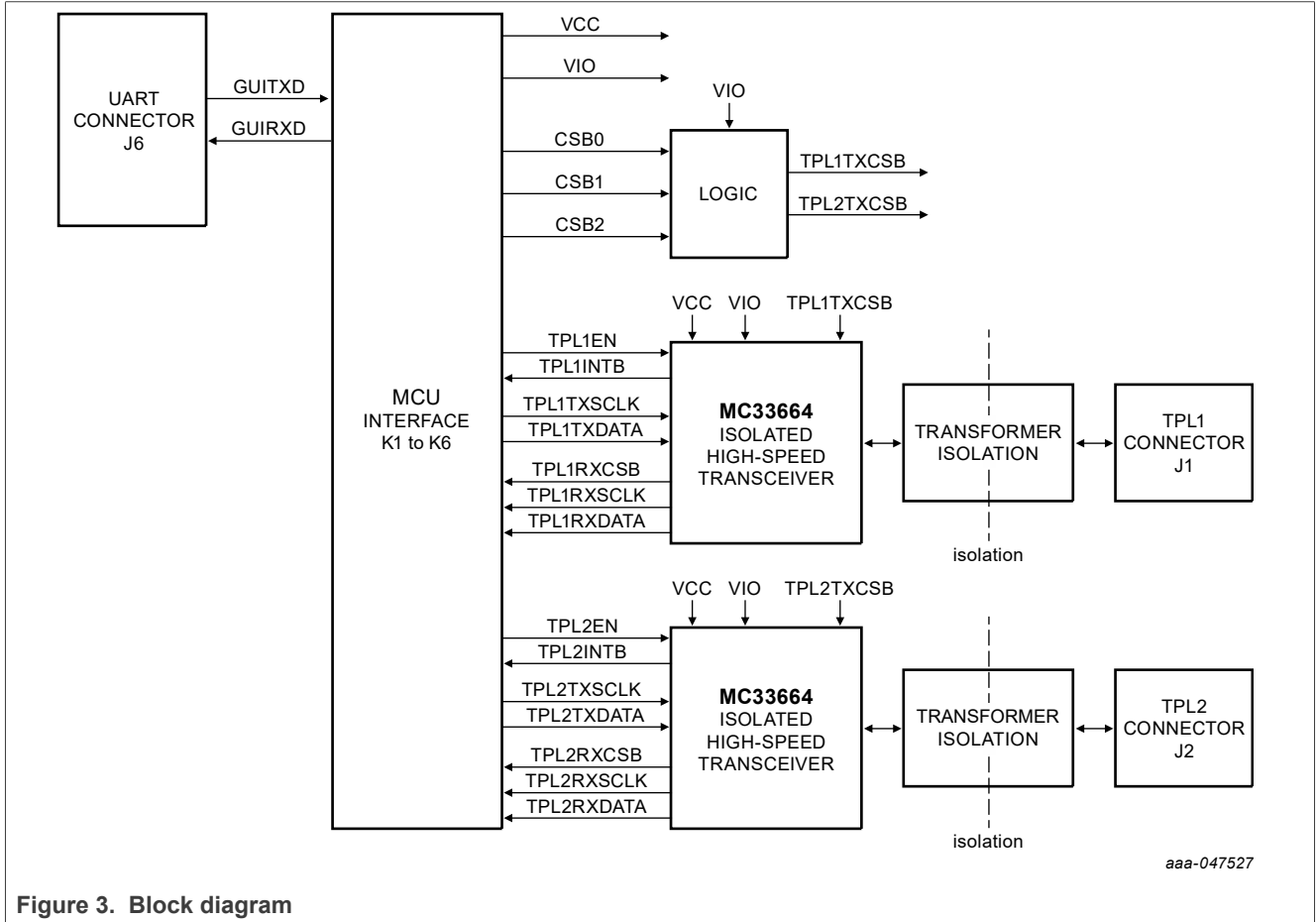
6.2.1.2 Block diagram

Figure 3. Block diagram

6.2.1.3 Features

- 2.0 Mbit/s isolated network communication rate
- Dual SPI architecture for message confirmation
- Robust conducted and radiated immunity with wake-up
- 3.3 V and 5.0 V compatible logic thresholds
- Low Sleep mode current with automatic bus wake-up
- Ultra-low radiated emissions
- Option to access UART of S32K344 via J6

6.2.1.4 Modes of operation

The modes of operation followed by MC33664 for the VIO and EN pins are shown in
Table 3.

Table 3. Modes of operation

Device mode	EN pin	VIO pin	Comment
Normal	1	1	The MC33664 operates as a full transceiver. MCU messages transmitted on the SPI_TX emerge on the SPI_RX for the MCU to read.
Sleep	0	1	In Sleep mode, the transceiver activates the INTB pin when a valid wake-up sequence is detected. The INTB pin remains LOW until the rising edge of the EN pin places the device in Normal mode.

6.2.2 Connectors
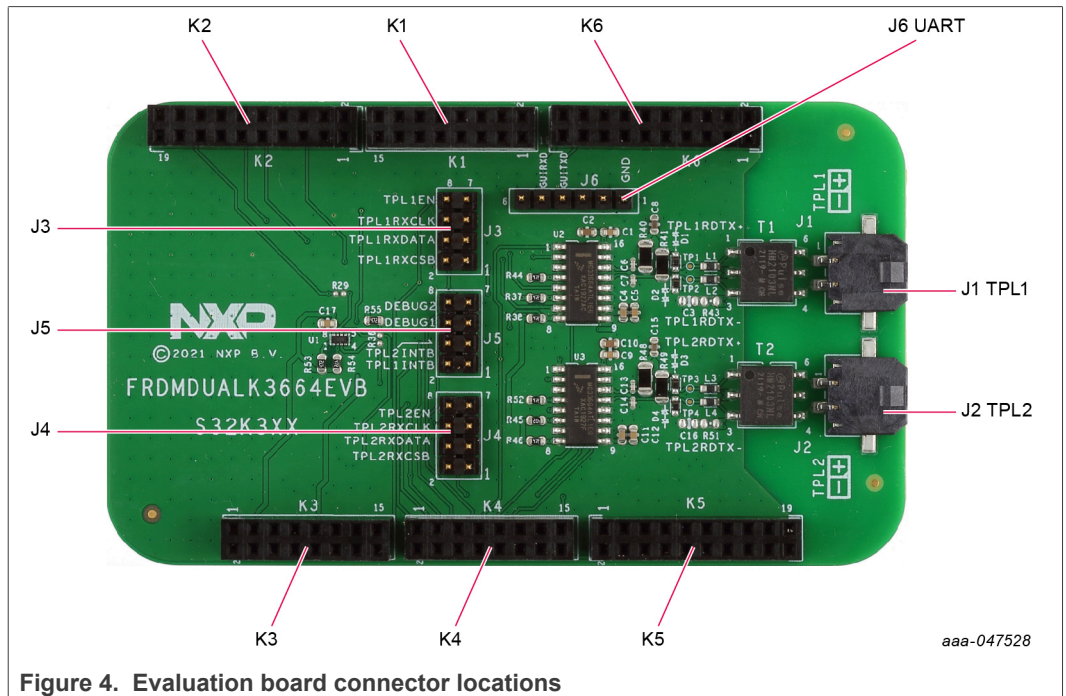
Figure 4 shows the location of connectors on the board.

Figure 4. Evaluation board connector locations

6.2.2.1 TPL bus connectors

The connectors J1 and J2 provide access to TPL1 and TPL2 bus.

Table 4. TPL bus 1 connector J1

Schematic label	Signal name	Description
J1-1	TPL1RDTXP	TPL bus 1 – receive/transmit input positive
J1-2	TPL1RDTXN	TPL bus 1 – receive/transmit input negative

Table 5. TPL bus 2 connector J2

Schematic label	Signal name	Description
J2-1	TPL2RDTXP	TPL bus 2 – receive/transmit input positive
J2-2	TPL2RDTXN	TPL bus 2 – receive/transmit input negative

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6.2.2.1.1   TPL bus selection

The FRDMDUALK3664EVB provides an option to select dynamically which TPL bus is addressed. Using three signals it is possible to transmit individually on the TPL1 or TPL2 bus, or to transmit simultaneously on both TPL1 and TPL2 bus.

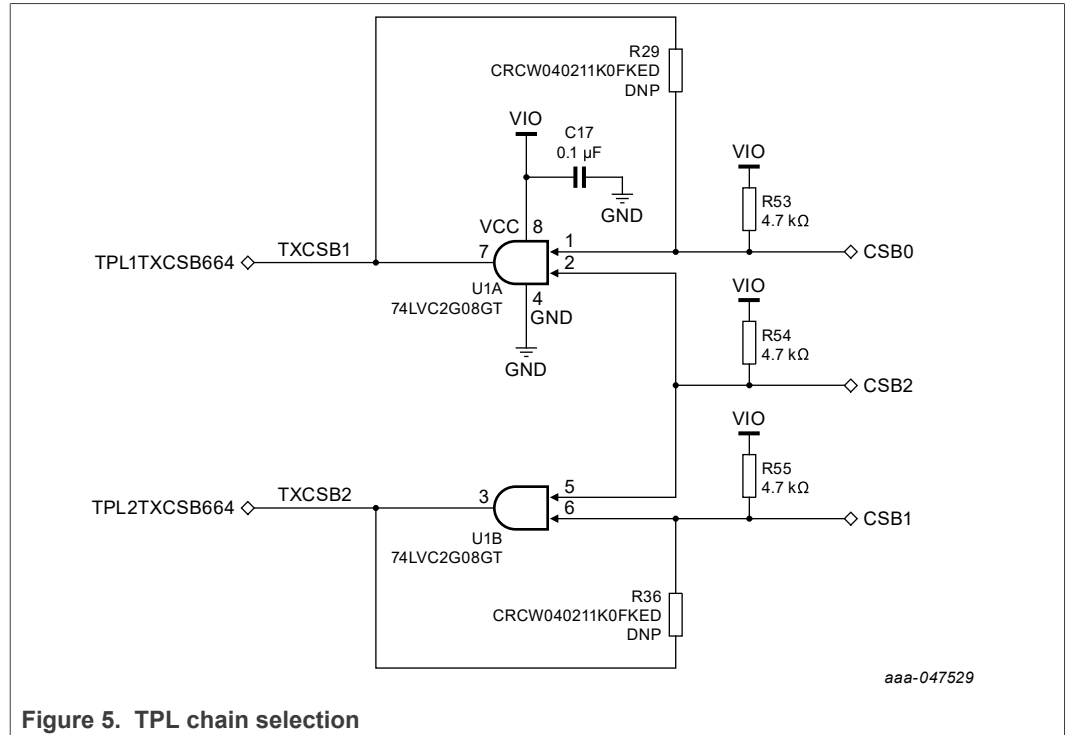*Note: For proper operation, the logic circuitry expects the unused CSB signals to be HIGH.*

Figure 5. TPL chain selection

Table 6. TPL bus selection

Selected CSB line (active LOW)	Selected TPL line (active LOW)
CSB0	TPL1
CSB1	TPL2
CSB2	TPL1 and TPL2

6.2.2.2   MCU interface connectors

The connectors K1 to K6 enable interface to an NXP microcontroller development platform. The mechanical dimensions and pinout are selected to fit the S32K3x4EVB-Q172 (recommended hardware platform).

Note: Connectors differ in number of rows. Only inner rows are used for easier stacking and unstacking.

Table 7 details the signals used for the S32K3x4EVB-Q172 evaluation boards.

Table 7. Signal routing for S32K3x4EVB-Q172

MCU interface	Signal	Description	Direction	MCU signal
K3-3	VIO	5.0 V IO supply	←	5V
K3-9	VCC5	5.0 V supply	←	5V
K3-11	GND	ground		GND
K3-13	GND	ground		GND
K5-12	GND	ground		GND
K2-13	GND	ground		GND
K6-12	GND	ground		GND
K4-2	TPL1EN	TPL1 enable	←	PTC19
K4-1	TPL1INTB	TPL1 interrupt	→	PTD1/EIRQ9
K4-4	TPL2EN	TPL2 enable	←	PTC18
K4-3	TPL2INTB	TPL2 interrupt	→	PTD0/EIRQ8
K2-17	TPL1TXCSB	TPL1 TX chip select	←	PTC6/LPSPI0_PCS1
K4-15	TPL2TXCSB	TPL2 TX chip select	←	PTE6/LPSPI0_PCS2
K2-19	TPL12TXCSB	TPL1 and TPL2 TX chip select	←	PTC7/LPSPI0_PCS0
K4-7	TPL12TXCLK	TPL1 and TPL2 TX clock	←	PTE1/LPSPI0_SCK
K4-13	TPL12TXDATA	TPL1 and TPL2 TX data	←	PTE2/LPSPI0_SOUT
K2-5	TPL1RXCSB	TPL1 RX chip select	→	PTB17/LPSPI1_PCS3
K2-11	TPL1RXCLK	TPL1 RX clock	→	PTB14/LPSPI1_SCK
K2-9	TPL1RXDATA	TPL1 RX data	→	PTB15/LPSPI1_SIN
K4-10	TPL2RXCSB	TPL2 RX chip select	→	PTC12/LPSPI2_PCS1
K4-6	TPL2RXCLK	TPL2 RX clock	→	PTB29/LPSPI2_SCK
K4-8	TPL2RXDATA	TPL2 RX data	→	PTB2/LPSPI2_SIN
K5-13	Debug1	GPIO for debugging purposes	←	PTE25
K5-15	Debug2	GPIO for debugging purposes	←	PTE26
K6-17	GUITXD	UART routed to connector J6 (UART)	→	PTE5/LPUART12_RX
K6-19	GUIRXD	UART routed to connector J6 (UART)	←	PTE4/LPUART12_TX

6.2.2.3 Logic analyzer interface connectors J3, J4, J5

These connectors are intended for software development and debugging purposes. They allow easy access to used signals and to monitor them, for instance, with a logic analyzer or an oscilloscope.

Table 8. Connector J3

Pin	Signal	Description
1	GND	ground
2	TPL1RXCSB	TPL1 RX chip select
3	GND	ground
4	TPL1RXDATA	TPL1 RX data
5	GND	ground
6	TPL1RXCLK	TPL1 RX clock
7	GND	ground
8	TPL1EN	TPL1 enable

Table 9. Connector J4

Pin	Signal	Description
1	GND	ground
2	TPL2RXCSB	TPL2 RX chip select
3	GND	ground
4	TPL2RXDATA	TPL2 RX data
5	GND	ground
6	TPL2RXCLK	TPL2 RX clock
7	GND	ground
8	TPL2EN	TPL2 enable

Table 10. Connector J5

Pin	Signal	Description
1	GND	ground
2	TPL1INTB	TPL1 interrupt
3	GND	ground
4	TPL2INTB	TPL2 interrupt
5	GND	ground
6	Debug1	optional debug signal
7	GND	ground
8	Debug2	optional debug signal

6.2.3 Compatible NXP MCU development platforms

FRDMDUALK3664EVB is compatible with the S32K3x4EVB-Q172 MCU development platform.

The information related to MCU development platform ordering and instruction is available at nxp.com.

6.2.4 UART connector J6

This connector is intended for USB to serial cable (for example, FTDI TTL-232R-5V).

Table 11. Connector UART J6

Pin	Signal	Description
1	GND	ground
2	-	not connected
3	-	not connected
4	GUITXD	connect to external UART TXD
5	GUIRXD	connect to external UART RXD
6	-	not connected

6.3 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the FRDMDUALK3664EVB evaluation board are available at http://www.nxp.com/FRDMDUALK3664EVB.

7 Configuring the hardware

The FRDMDUALK3664EVB is configured as a shield board for the S32K3x4EVB-Q172 board. It can also be used in a standalone configuration. For other configurations, check mechanical and electrical fit or use, for example, a breadboard design.

7.1 S32K3x4EVB-Q172 board configuration

The FRDMDUALK3664EVB is configured for the S32K3x4EVB-Q172 board by default. Ensure that the S32K3x4EVB is configured correctly before connecting both boards together.

Table 12 lists the relevant S32K3x4EVB-Q172 configurations required with the FRDMDUALK3664EVB. All other settings should use the default settings. For further details, consult the S32K3x4EVB-Q172 board user manual[3].

Table 12. S32K3x4EVB-Q172 recommended setting

Jumper	Configuration	Description
J18	1-2	VDD_HV_A = 5 V
J19	2-3	VDD_HV_B = VDD_HV_A

When both boards are connected, the SPI and other signals are directly connected with suitable MCU pins. Power is supplied to the FRDMDUALK3664EVB through the 5.0 V from the S32K3x4EVB.

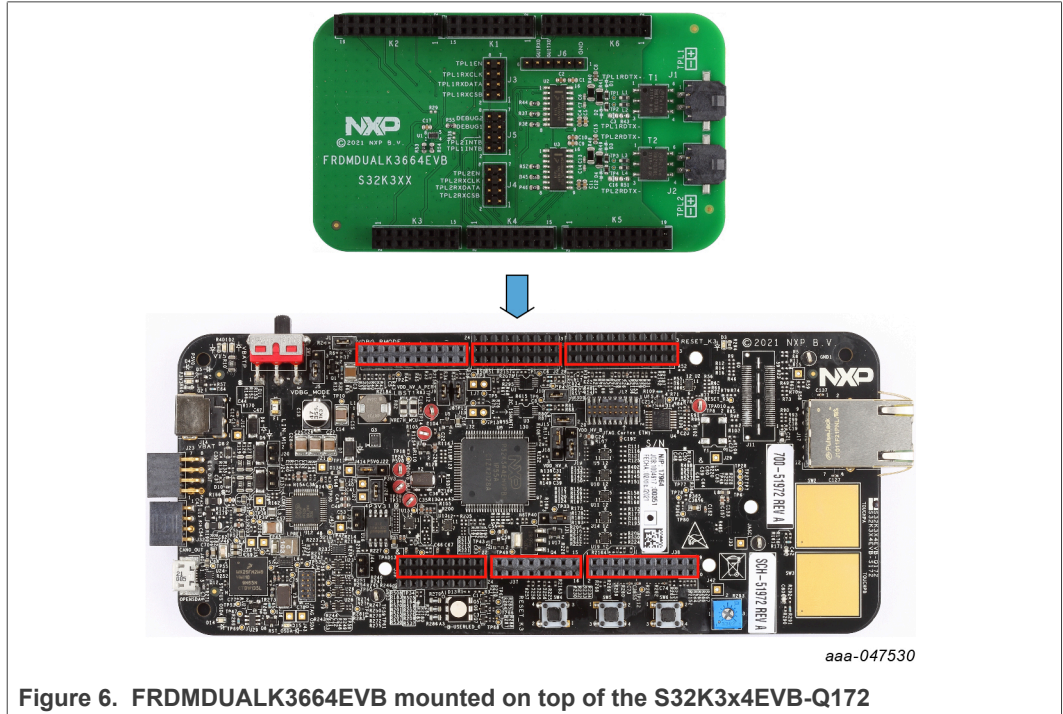*Note:* *The S32K3x4EVB-Q172 requires an external 12 V 2 A power supply.*

Figure 6. FRDMDUALK3664EVB mounted on top of the S32K3x4EVB-Q172

7.2 Standalone or other microcontroller platforms

When the board is used in standalone or with other microcontroller platforms, the SPI signals must be manually connected to the MCU interface connectors according to Table 7.

Required power supply connections are:

- VCC5 must be provided with 5.0 V
- VIO must be provided with 3.3 V or 5.0 V depending on the required communication signal levels

8 References

[1] **FRDMDUALK3664EVB** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/FRDMDUALK3664EVB

[2] **MC33664** — product information on MC33664, isolated network high-speed transceiver
http://www.nxp.com/MC33664

[3] **S32K3x4EVB-Q172** — detailed information on this board, including documentation, downloads, and software and tools
https://www.nxp.com/S32K3X4EVBQ172

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