An Example MPC8540-Based CompactPCI Reference Design

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CompactPCI™ is a very high performance industrial bus based on the standard PCI electrical specification in a rugged 3U or 6U Eurocard packaging.Compared to standard desktop PCI, CompactPCI supports twice as many PCI slots (8 versus 4) and offers a packaging scheme that is much better suited for use in industrial applications.Due to its extremely high bandwidth, the CompactPCI bus is particularly well suited for many high speed data communication applications such as servers, routers, converters and switches. Full CompactPCI specifications are available from the PCI Industrial Computer Manufacturers Group at www.picmg.org.

This White Paper describes an example design of a compact PCI reference system based on the latest MPC8540 integrated PowerPC™ processor.

Contents

1 Introduction

The MPC8540 is a member of the latest PowerPC processor based family of integrated devices. It is based on a 32-bit implementation of the “new” Book E Embedded PowerPC processor core. This core is known as the e500 core and supports the features detailed in the PowerPC Book E architecture definition.

This core has several features that differ from other PowerPC cores which are known as “Classic PowerPC.” Details of the differences are described in a separate Application Note.

The key features of the MPC8540 are described in the MPC8540 User's Manual and therefore will not be repeated here.

The device consists of the following components in a 783-ball FC-PBGA package

- Embedded e500 Book E-compatible core
- 256 Kbytes of on-chip memory
- DDR memory controller
- Local Bus Controller
- 2 x Three-speed (10/100/1000) Ethernet controllers (TSEC)
- RapidIO interface unit
- PCI/PCI-X functional unit
- Integrated DMA controller
- Programmable Interrupt Controller (PIC)
- DUART
- I2C Controller
- Boot sequencer
- Address translation and mapping unit (ATMU)
- System performance monitor
- System access port
- Power management
- IEEE 1149.1-compliant, JTAG boundary scan

A block diagram of the main functional units within the MPC8540 is shown in Figure 1.

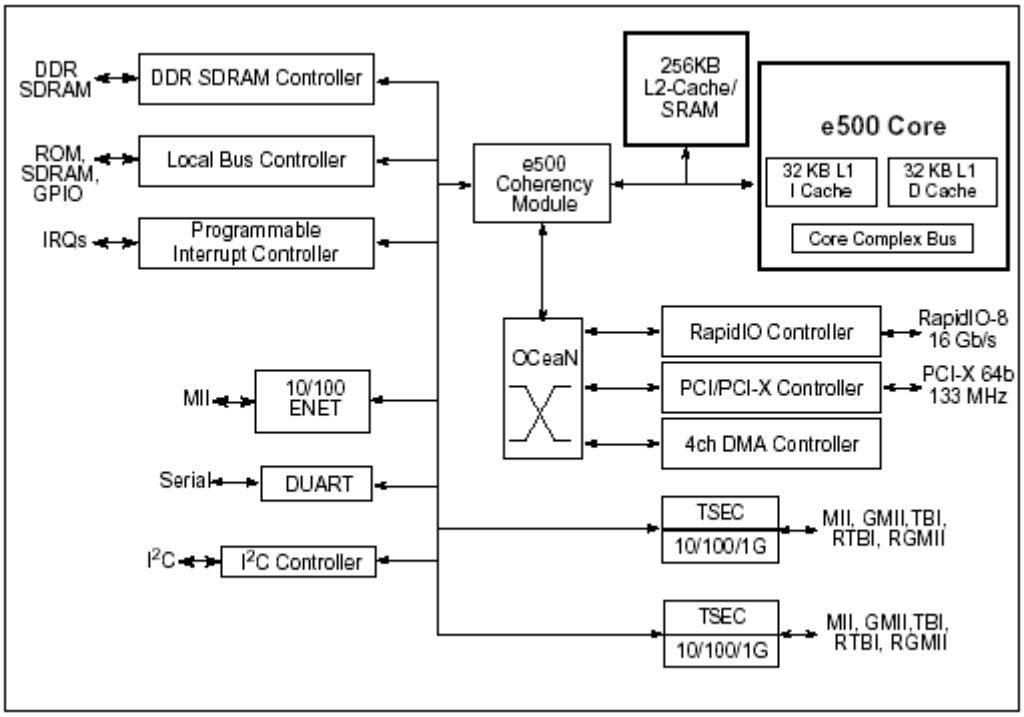

Figure 1. MPC8540 Functional Block Diagram

2 Example Reference CompactPCI Design

This example reference design utilises the on chip PCI Controller in the MPC8540 to interface to the CompactPCI bus. It contains a block of DDR SDRAM memory which is controlled directly by the device and a small amount of Flash memory used to hold power on reset boot code.

One of the TSEC ethernet interfaces is brought out to a standard RJ-45 socket via a Gb Ethernet PHY device and associated interface logic. Separate debug interface ports are provided via the on-chip DUART interface.

The RapidIO Trade Association have defined a standard interface connector for a parallel RapidIO interface. This forms part of the specification for a Hardware Implementation Platform (HIP) which allows standard PCI to RapidIO inter operability. This HIP platform is not defined for CompactPCI systems. For reference purposes the schematics for this example design show this standard RapidIO connector as an optional extra connector.

Full details are available at www.rapidio.org.

3 Block Diagram of Example Reference Design

A block diagram of the example system is shown in Figure 2.

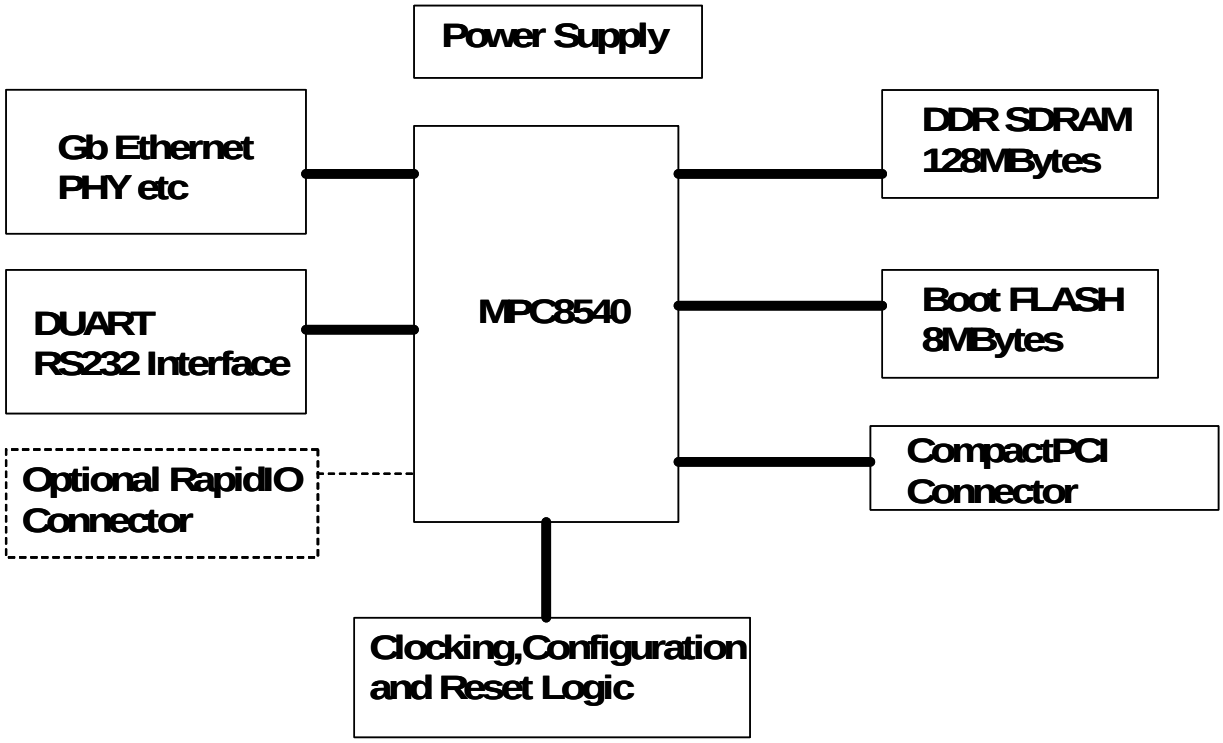

Figure 2. Block Diagram of Reference Design

3.1 MPC8540

The MPC8540 is the processing element of this design. It contains a 32-bit embedded PowerPC processor core and interfaces to each of the other blocks of this example reference design.

3.2 DDR SDRAM

The main memory array is built from 5 x MT46V16M16 DDR SDRAM devices. These are configured to provide 128MBytes of 64-bit wide memory along with one parity bit for each memory byte. The control of the DDR memory system is handled by the DDR memory controller implemented within the MPC8540 device.

3.3 Boot Flash

The boot Flash is implemented by a single 8MByte AMD29L_V641D device configured to be 16-bits wide. Since the local bus of the MPC8540 is a multiplexed address and data bus, an external latch using 74LVT16373 devices is implemented and controlled by the Local Address Latch Enable (LALE) signal from the MPC8540.

3.4 Compact PCI Connectors

The MPC8540 device contains an on-chip PCI/PCI-X interface which handles all the defined protocol for these buses. The PCI bus is brought out to two separate edge connectors on the board which conform to the Compact PCI interface specification. These are the connectors defined as J1 and J2 in the CompactPCI specification. Note the MPC8540 only supports 3.3V I/O. If a 5V interface is to be supported then level shifting logic will be required between the MPC8540 and the connectors.

3.5 Gb Ethernet PHY

The MPC8540 contains a two separate triple speed ethernet controllers which support speeds of 10Mbps, 100Mbps and 1Gbps. One of these controllers is brought out to an RJ45 edge connector via a Marvell 88E1011Gb Ethernet physical transceiver device

3.6 DUART

The MPC8540 also contains a dual UART interface that supports simple serial interfaces. These channels are brought out to 9-way D type RS232 connectors. These ports would be typically be used for debug and maintenance work

3.7 Clocking, Configuration and Reset Logic

The MPC8540 uses the input 66MHz PCI clock as a reference and makes use of on-chip PLLs to multiply this clock frequency to drive the memory interface bus and processor core. A diagram of the clock structure is shown in Figure 3.

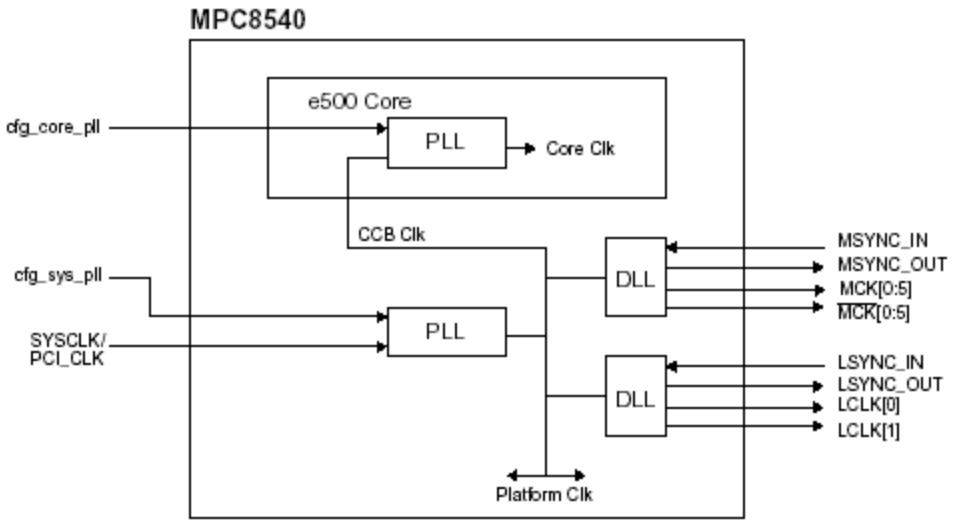

Figure 3. Clock sub-system Block Diagram

Many of the features of the MPC8540 are configured by sampling a series of pins during reset. In this reference design the configuration pins are all implemented as a series of small DIP switches that are configured by hand before the device is reset. For a design where the final configuration is known at the design stage then these DIP

switches can be omitted and replaced by pull-up or pull-down resistors to achieve the desired value on the configuration pins.

3.8 Power Supply

Assuming this board will be supplied with +5V and +3.3V from the CompactPCI backplane then all the other voltages required on the board are generated by the various power convertor circuits on the card. This includes 2.5V for the DDR memory and Ethernet PHY. The 1.2V cpu core voltage and the 1.5V for the Ethernet PHY. The 1.25V reference voltage for the DDR memory is produced by the LP2995 DDR voltage regulator device.

4 Example Interface Schematics

A full set of interface schematics are shown below. These were created using OrCad version 9.2 available from Cadence Design Systems™. The schematics are laid out in a hierarchical sequence of sheets.

The following pages give a full set of example schematics for an MPC8540 Compact PCI Reference design. They also include an optional RapidIO connector.

The schematics are laid out in a hierarchical fashion as follows:

Table 1. Top Level System Interconnection

Figure 4	Top Level System Interconnection
Figure 5	Top Level view of MPC8540 and memory systems
Figure 6	DDR SDRAM Memory Array
Figure 7	MPC8540 Top Level
Figure 8	Boot FLASH Memory
Figure 9	MPC8540 CPU and Local Bus Interface
Figure 10	MPC8540 DDR SDRAM Interface
Figure 11	DDR SDRAM Termination
Figure 12	MPC8540 Gb Ethernet Interface
Figure 13	MPC8540 RapidIO Interface
Figure 14	MPC8540 Power on Configuration Logic
Figure 15	MPC8540 PCI/PCI-X Interface
Figure 16	MPC8540 Parallel I/O and DUART Interface
Figure 17	MPC8540 Power Connections
Figure 18	Compact PCI J1 and J2 Connectors
Figure 19	Clock and Reset Logic
Figure 20	Local Power Supply Logic
Figure 21	Gb Ethernet Transceiver
Figure 22	RS232 Interface Logic
Figure 23	Optional RapidIO Connector
Figure 24	MPC8540 COP Debug Connector

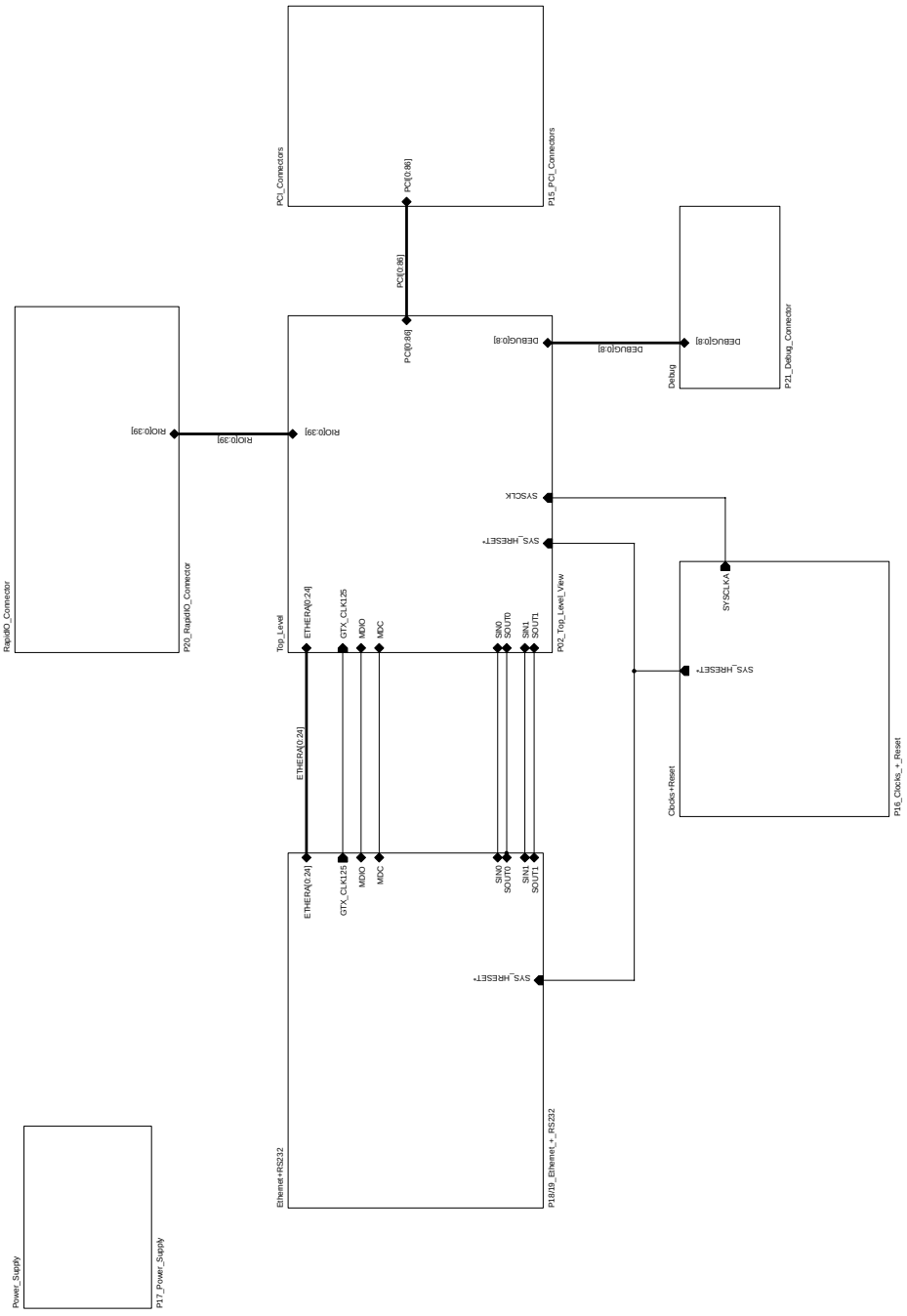

Figure 4. Top Level System Interconnection

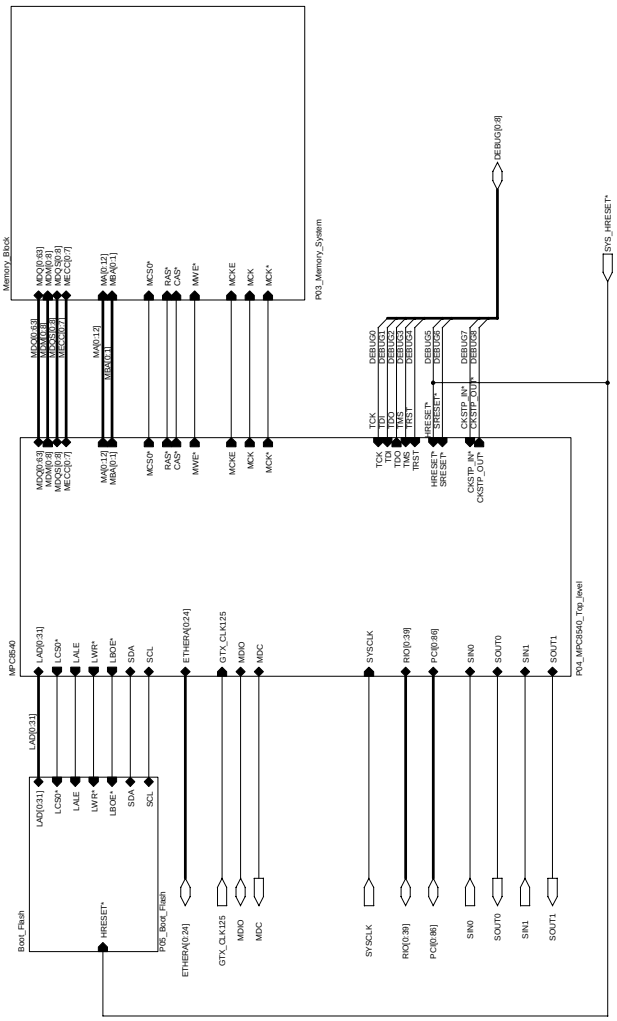

Figure 5. Top Level view of MPC8540 and memory systems

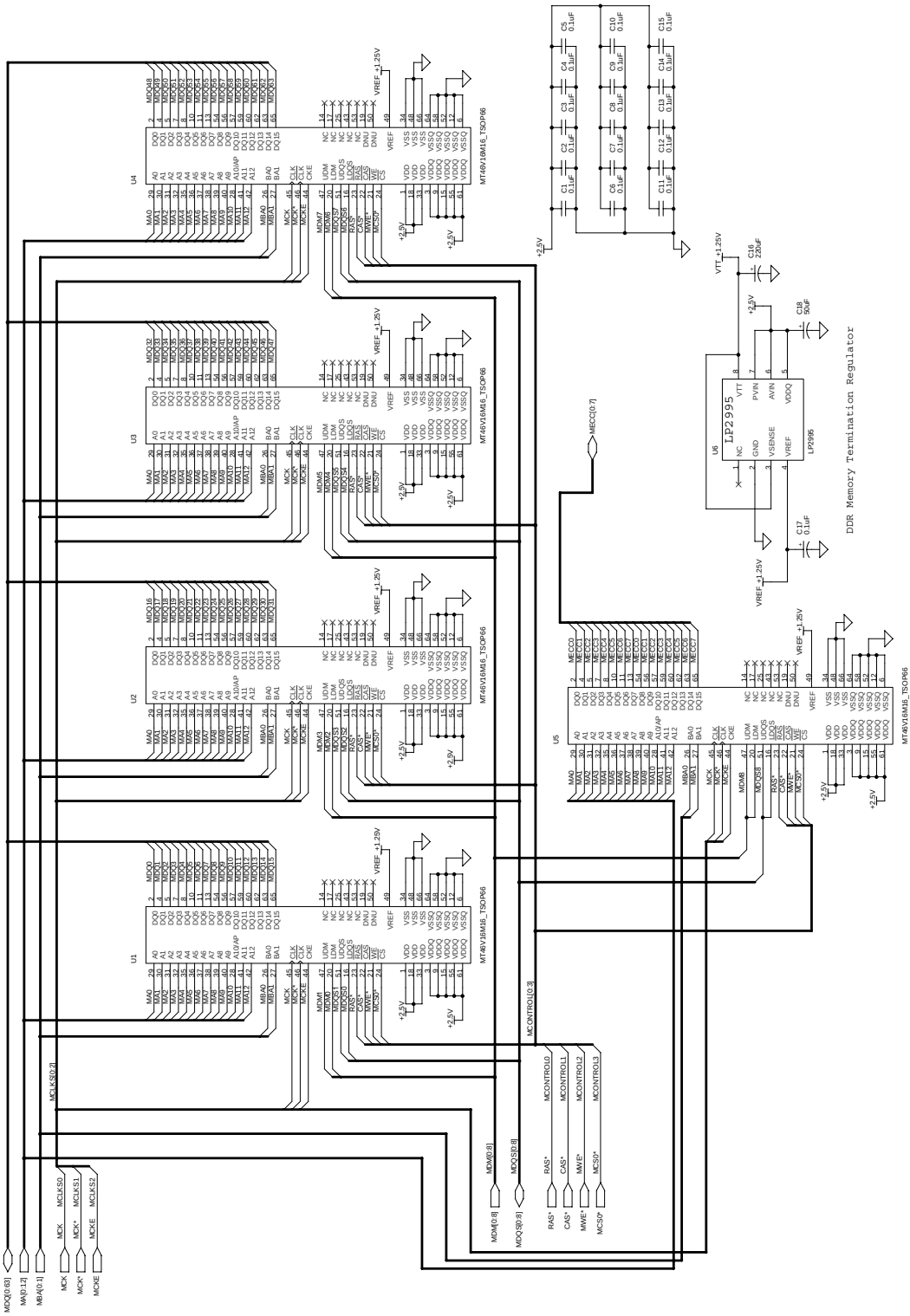

Figure 6. DDR SDRAM Memory Array

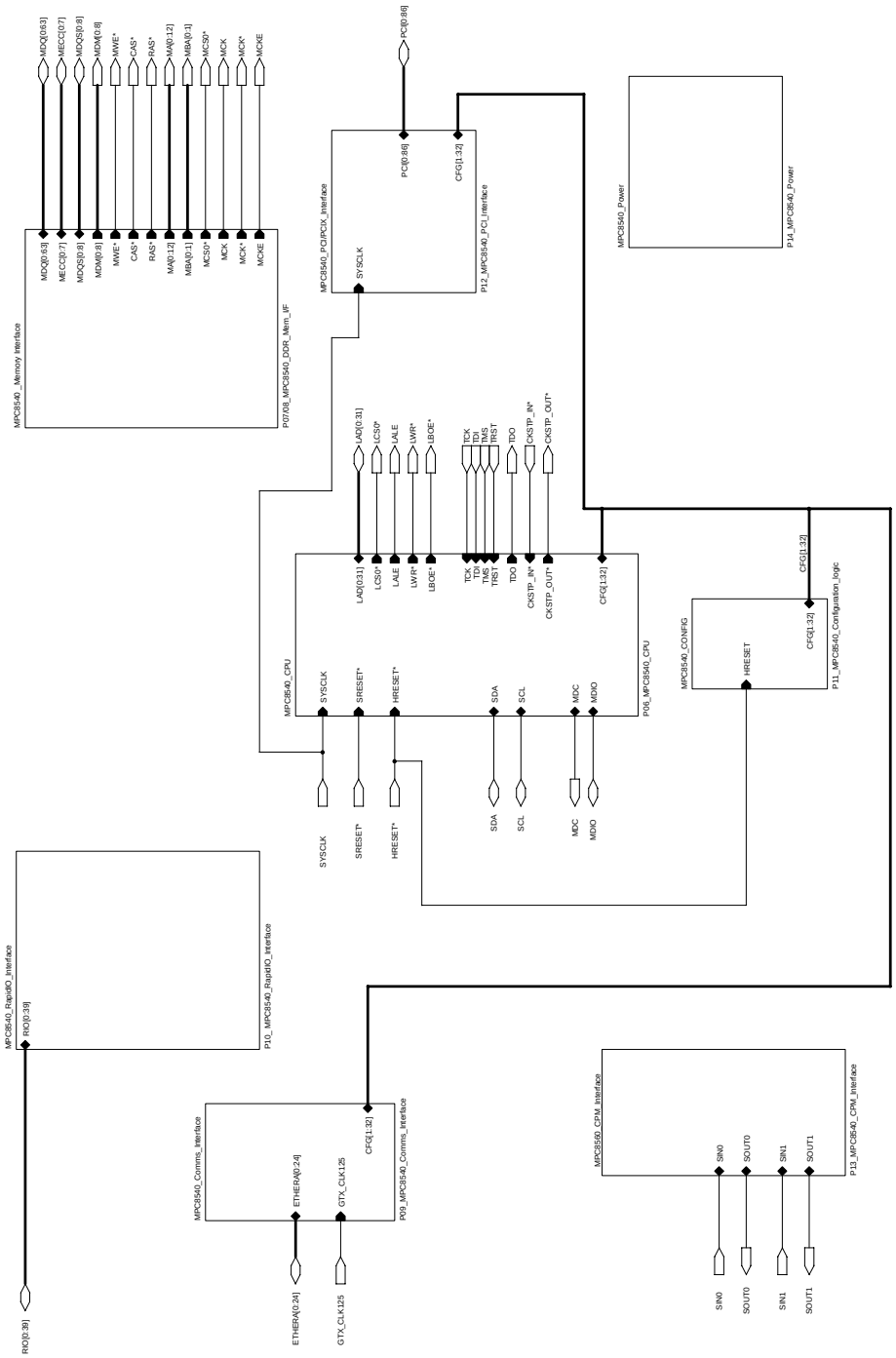

Figure 7. MPC8540 Top Level

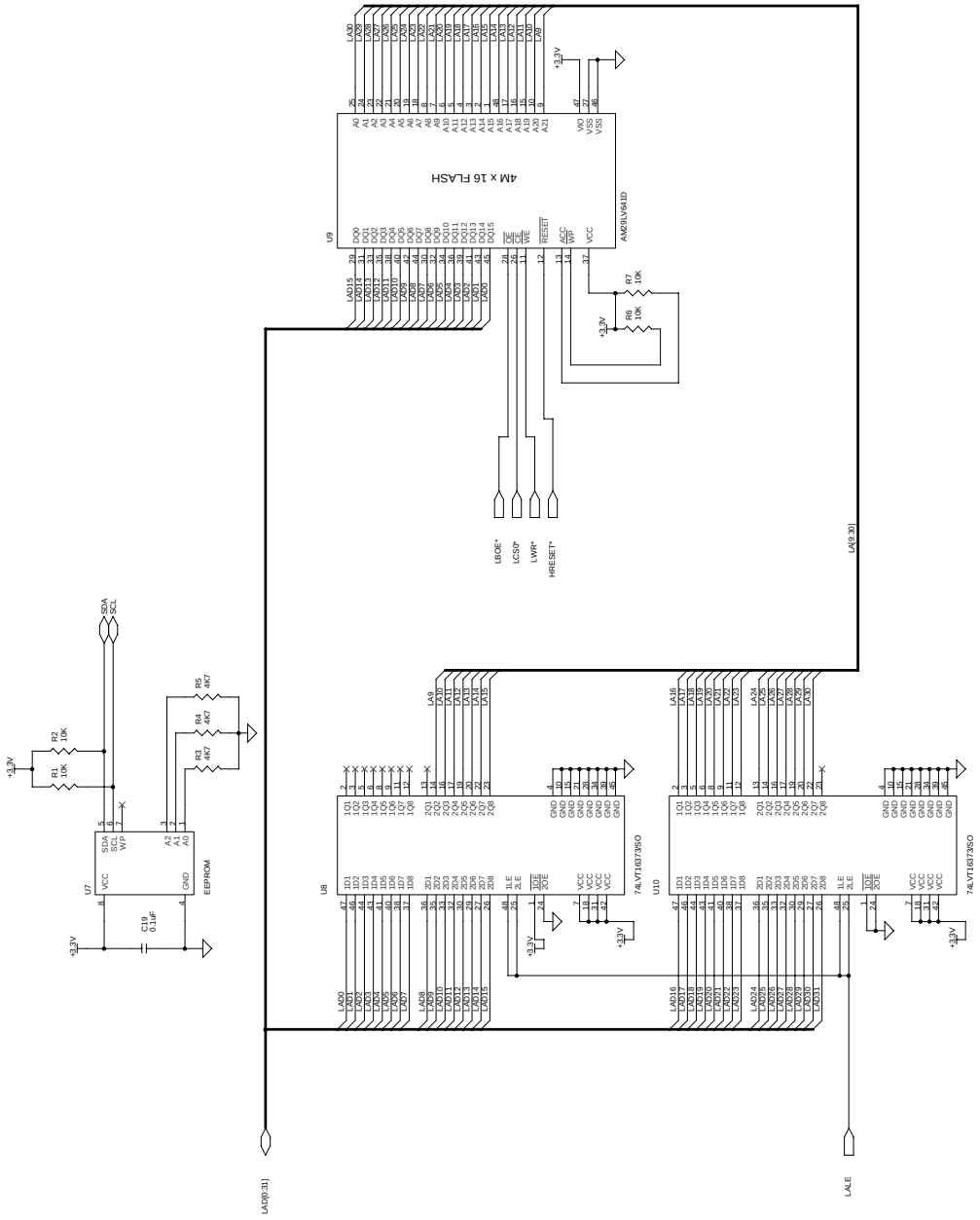

Figure 8. Boot FLASH Memory

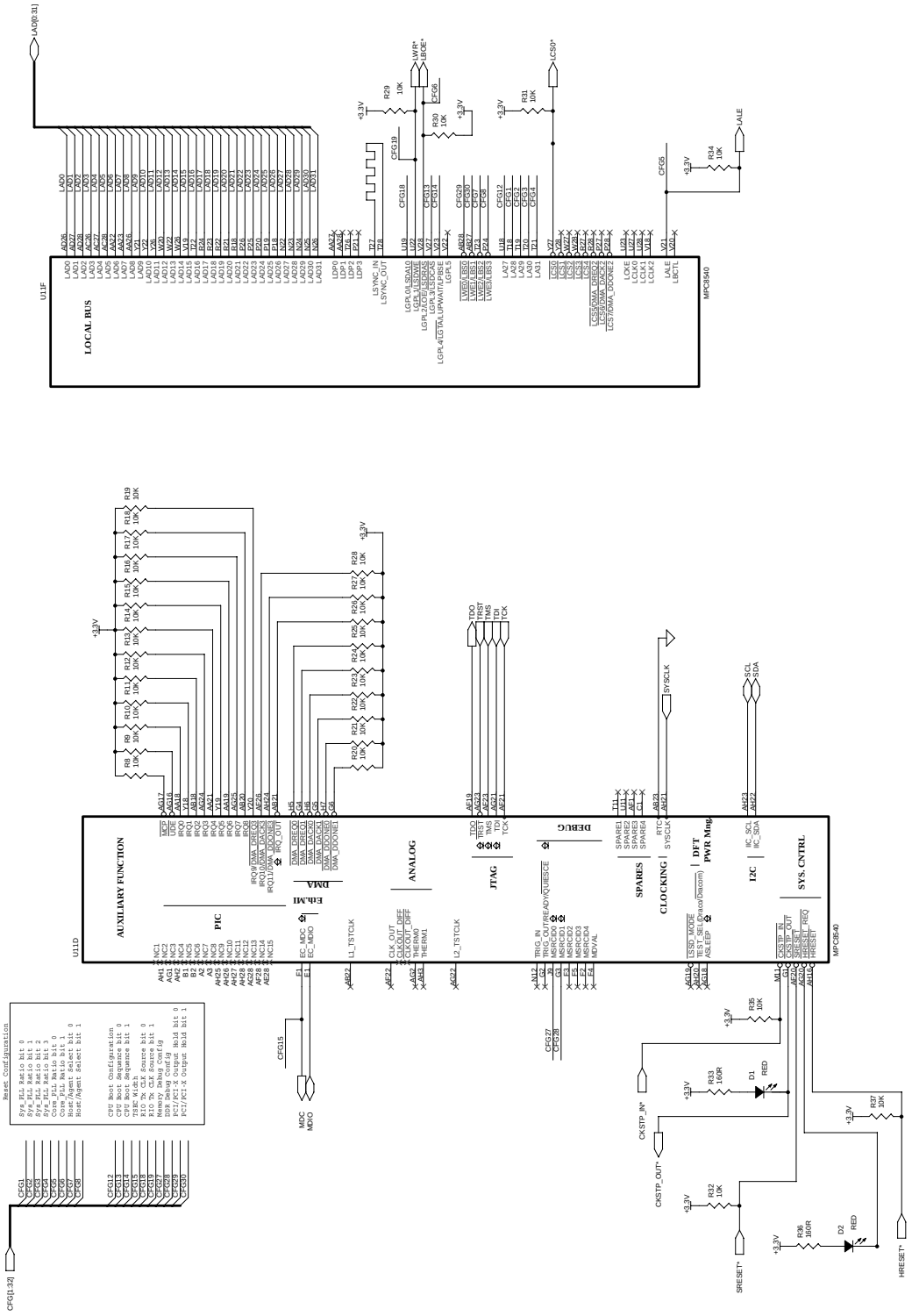

Figure 9. MPC8540 CPU and Local Bus Interface

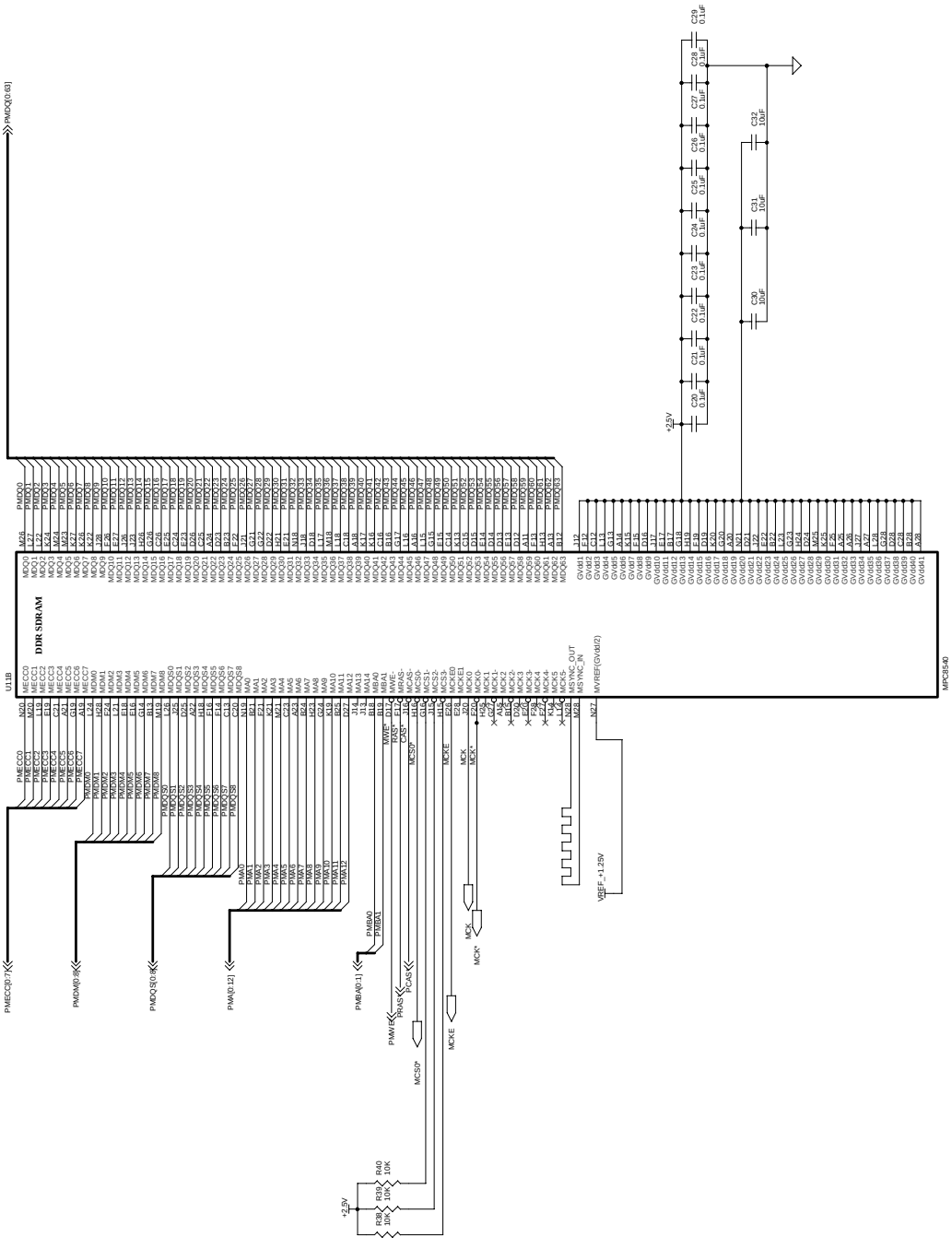

Figure 10. MPC8540 DDR SDRAM Interface

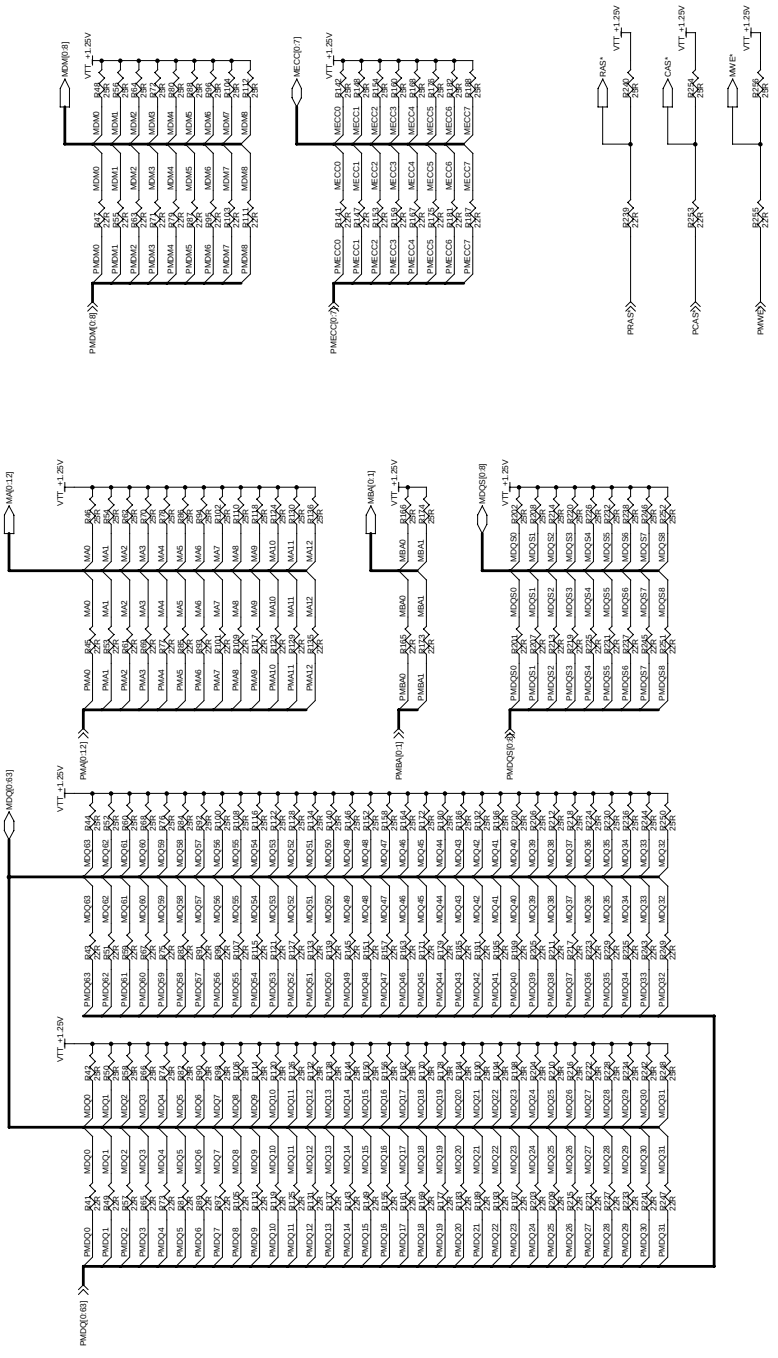

Figure 11. DDR SDRAM Termination

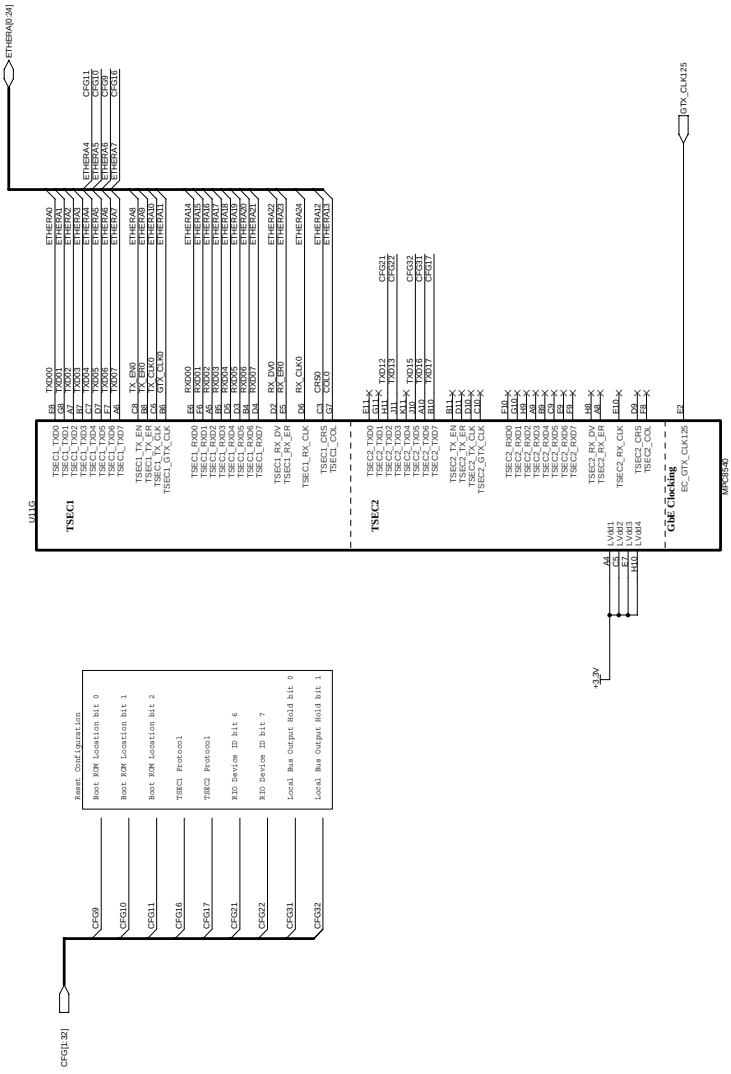

Figure 12. MPC8540 Gb Ethernet Interface

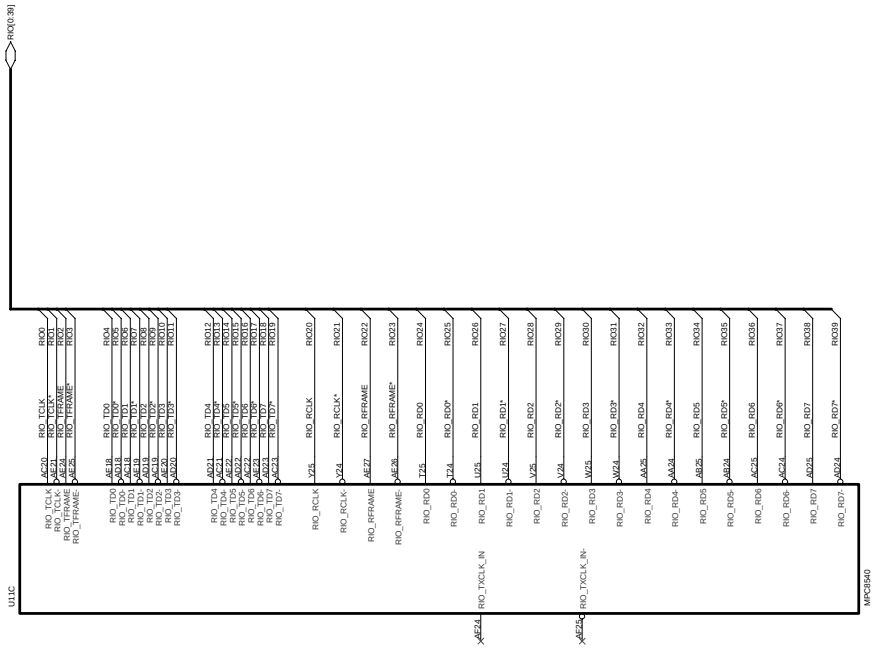

Figure 13. MPC8540 RapidIO Interface

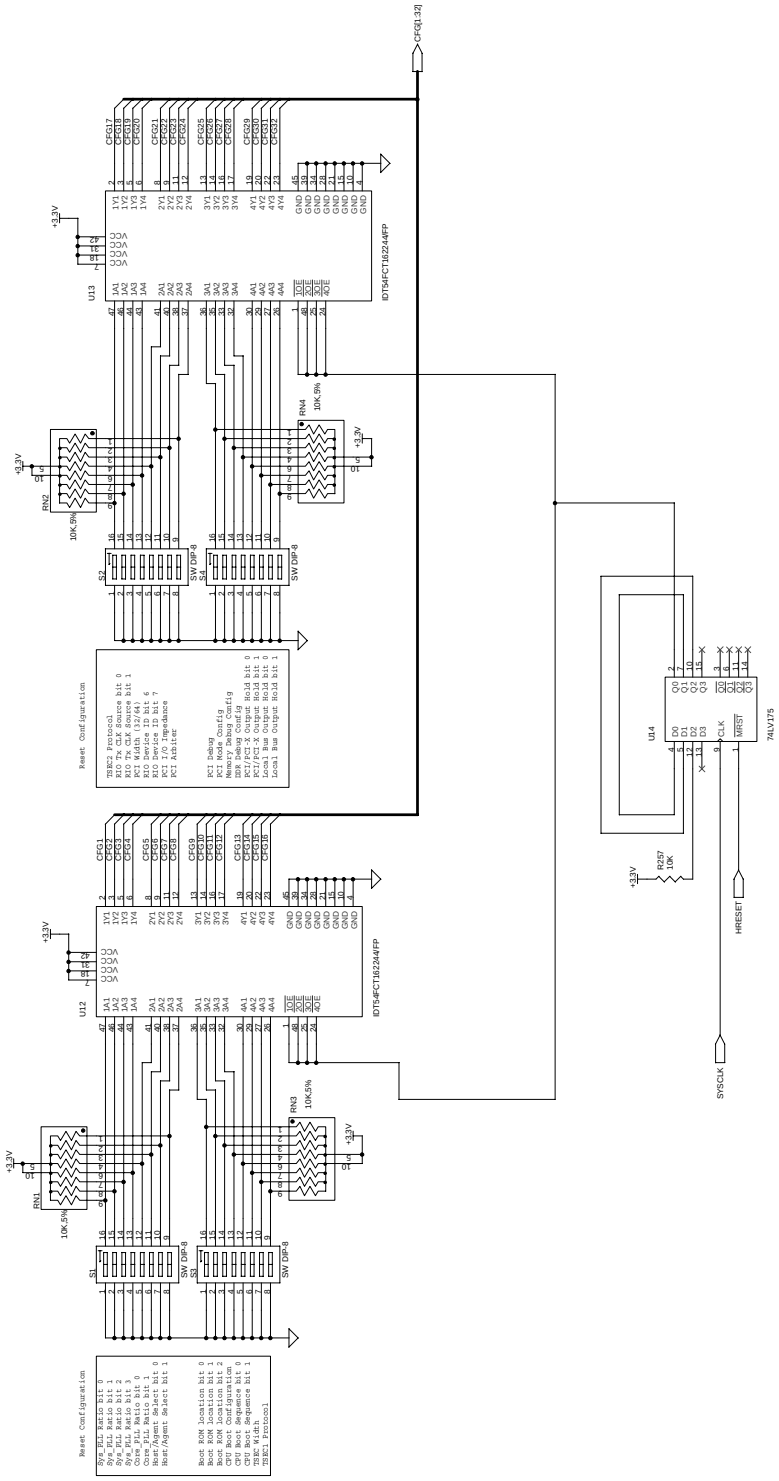

Figure 14. MPC8540 Power on Configuration Logic

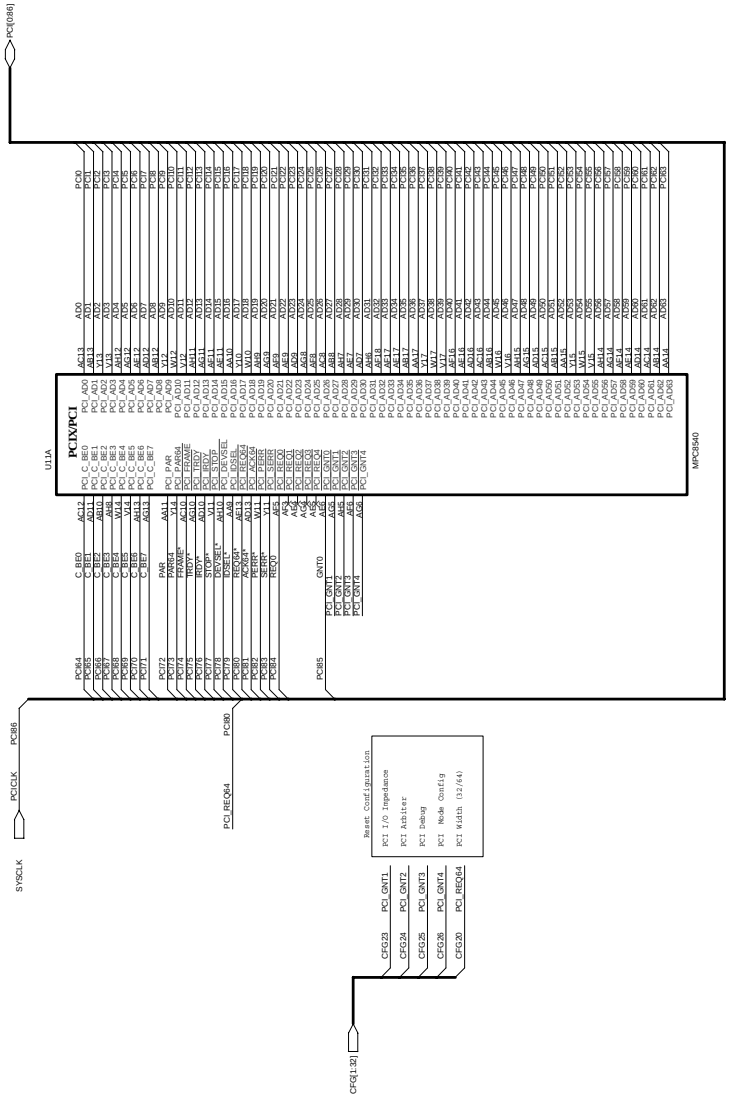

Figure 15. MPC8540 PCI/PCI-X Interface

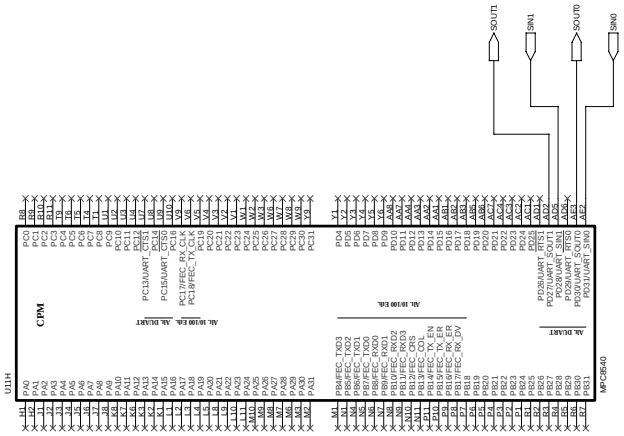

Figure 16. MPC8540 Parallel I/O and DUART Interface

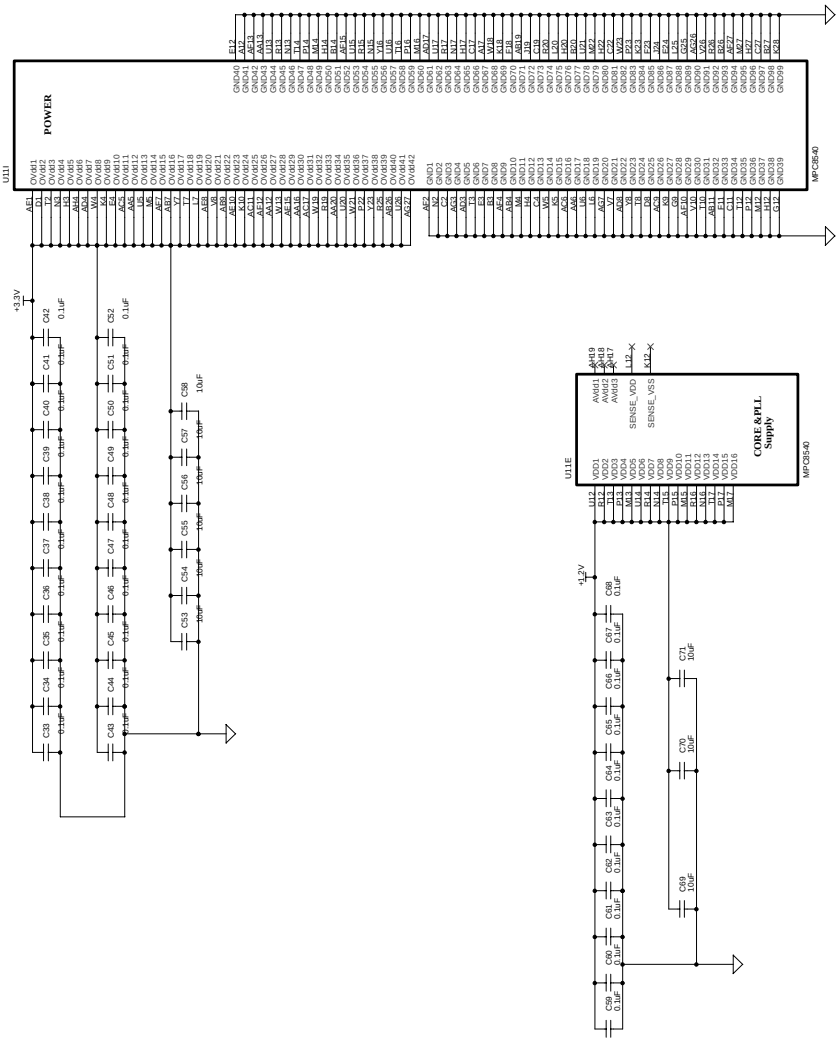

Figure 17. MPC8540 Power Connections

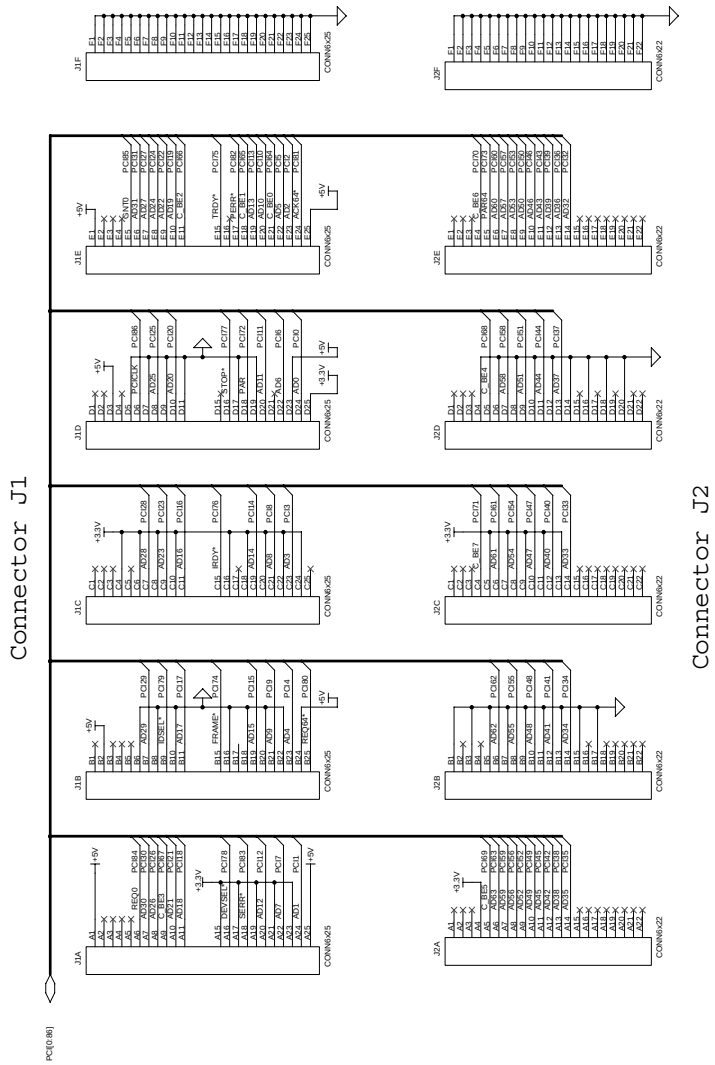

Figure 18. Compact PCI J1 and J2 Connectors

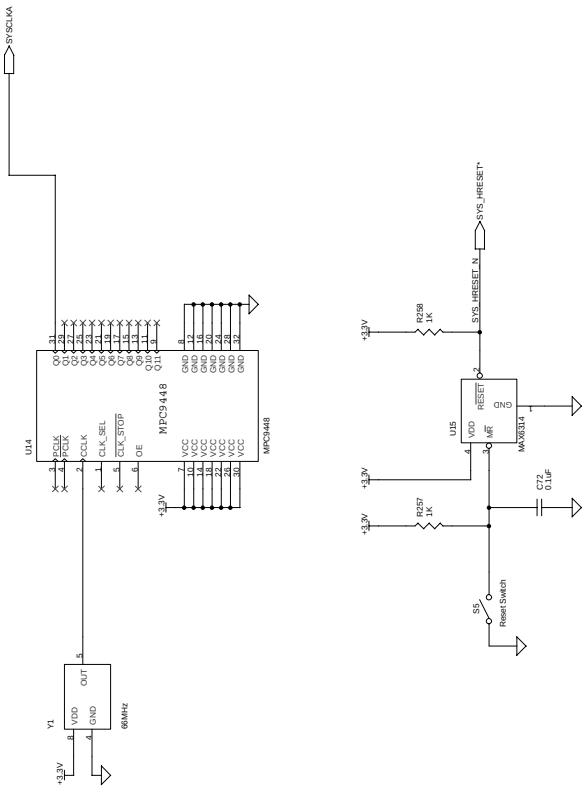

Figure 19. Clock and Reset Logic

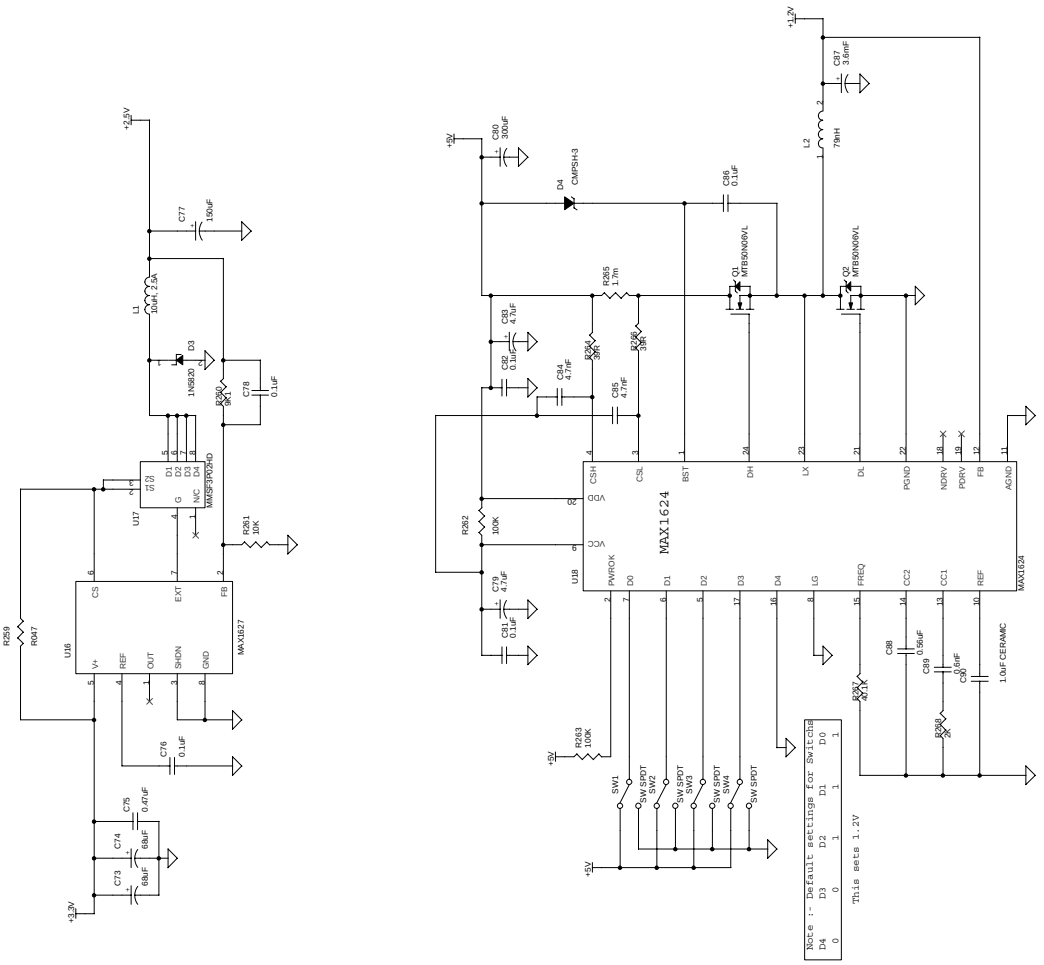

Figure 20. Local Power Supply Logic

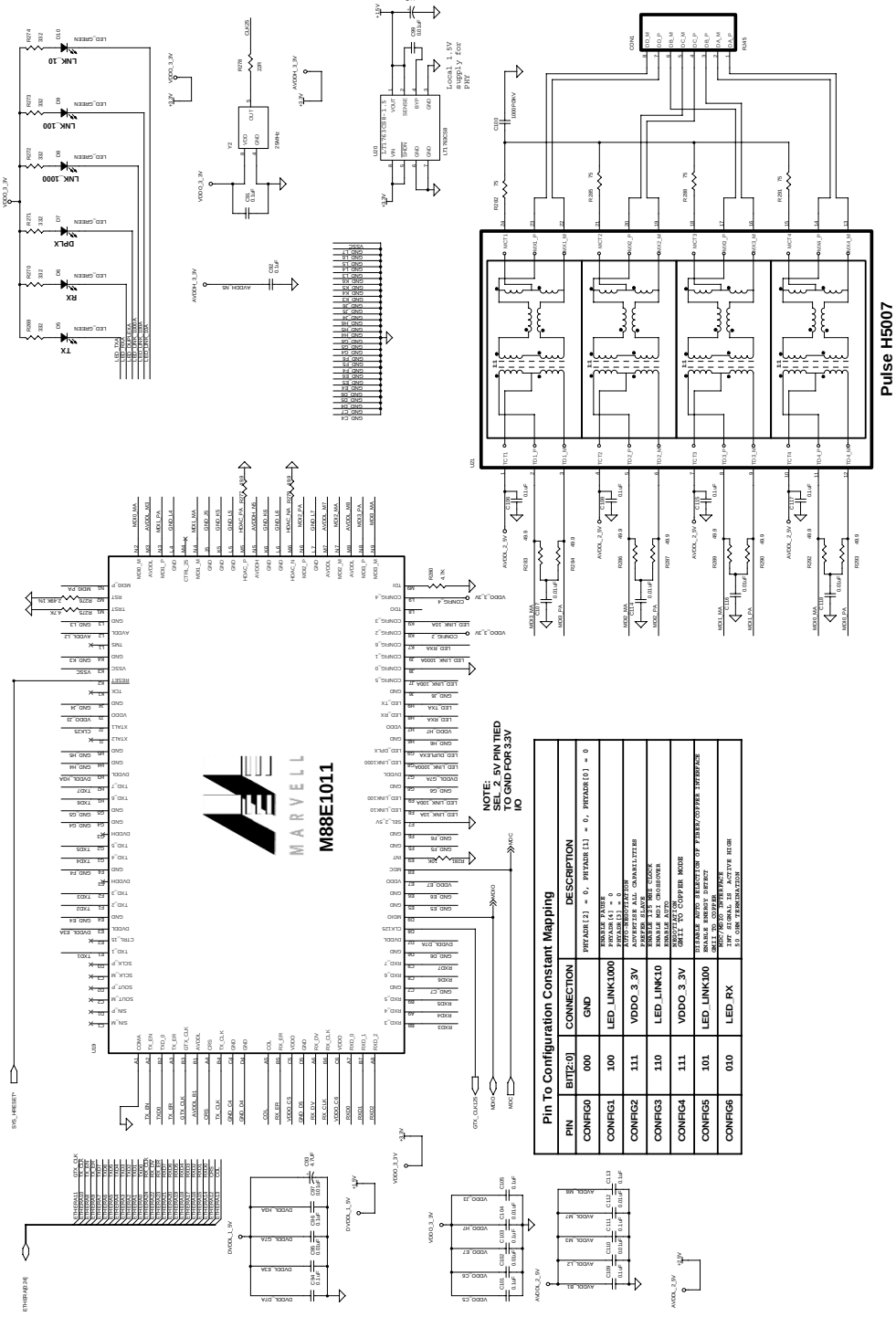

Figure 21. Gb Ethernet Transceiver

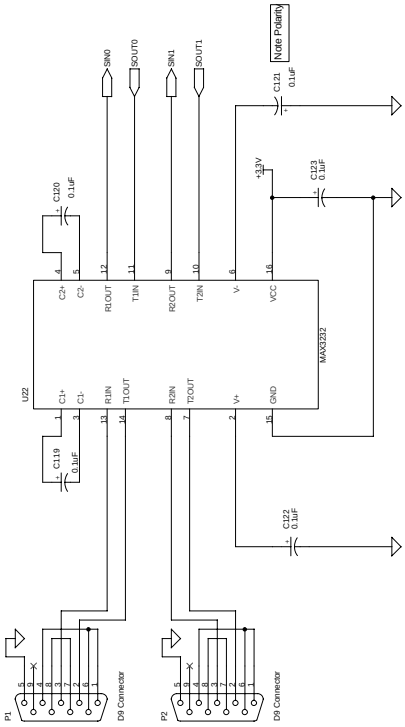

Figure 22. RS232 Interface Logic

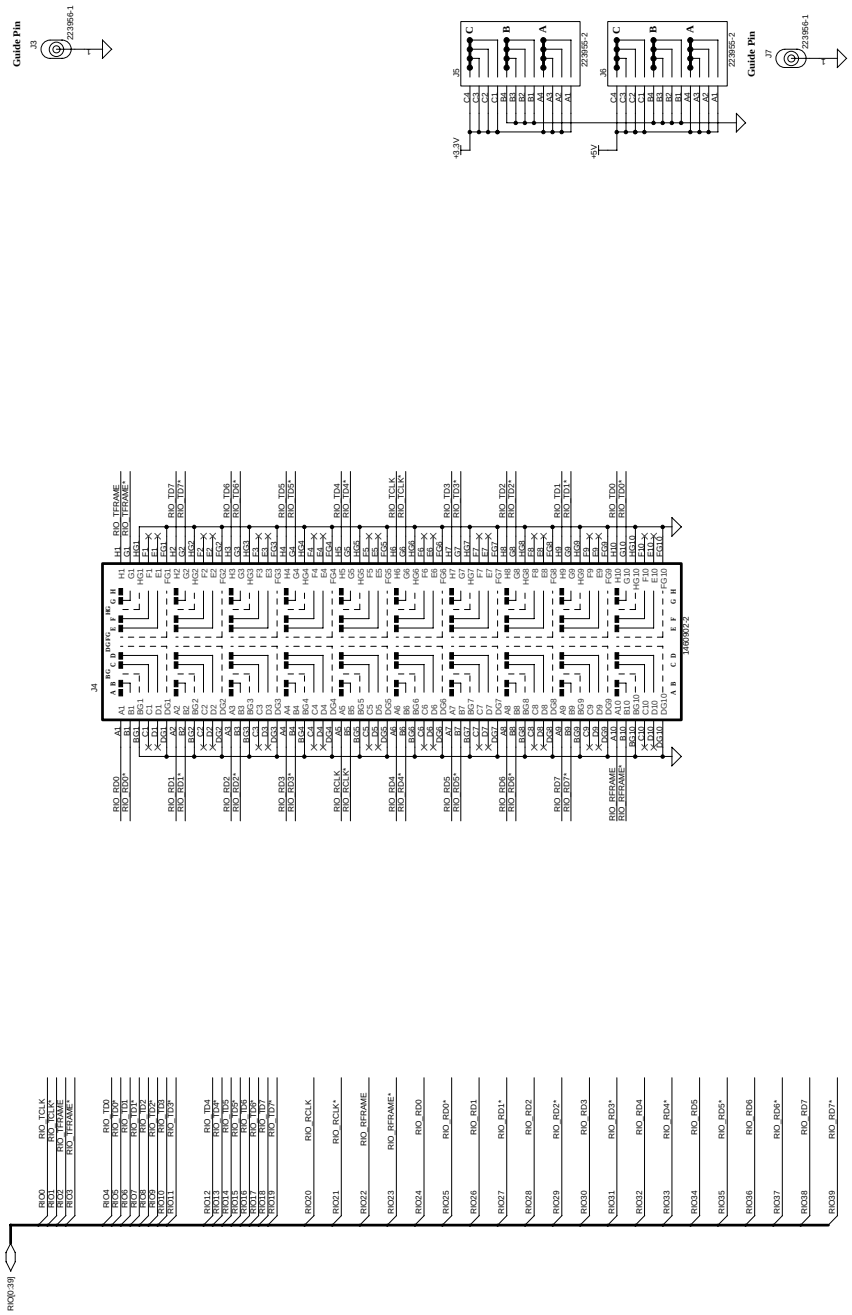

Figure 23. Optional RapidIO Connector

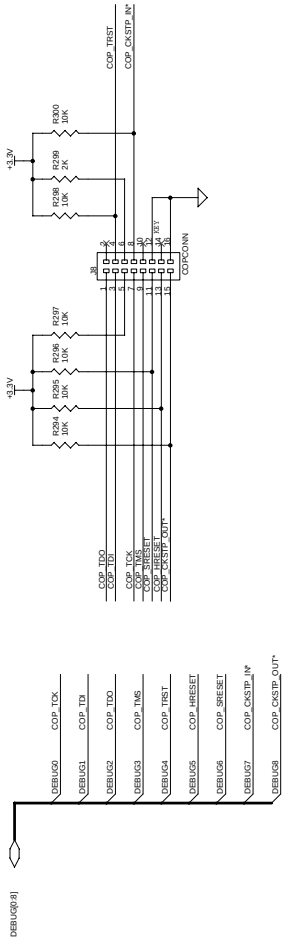

Figure 24. MPC8540 COP Debug Connector

5 Document Revision History

Table 2 provides a revision history for this white paper.

Table 2. Document Revision History

Revision	Date	Change(s)
1	11/2004	Template update. Updated schematics related to DDR hook-up.
0	8/2003	Initial release.

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