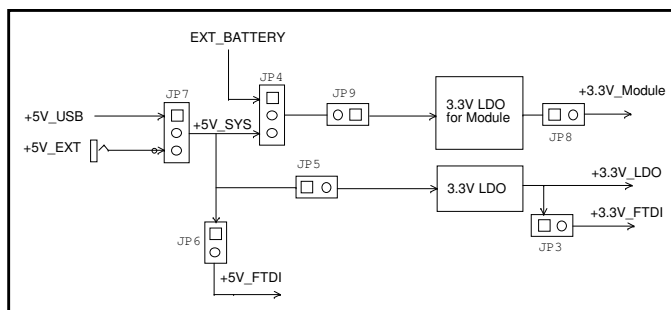
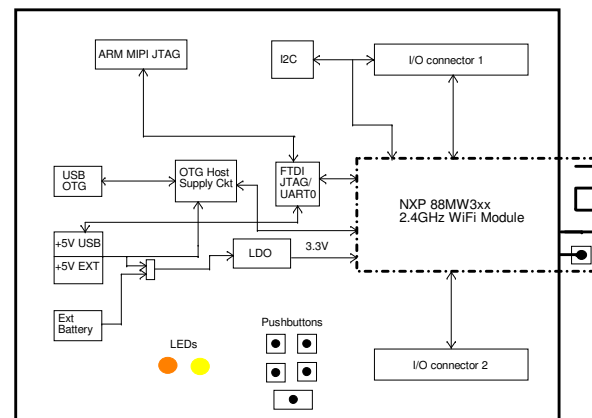


# NXP SEMICONDUCTORS

## Power Distribution



## Block Diagram



## Table of Contents

1. Power Distribution, Block Diagram
2. Power, Module Interface, Pin Muxing
3. FTDI- JTAG UART, USB OTG, MCI JTAG, MFI
4. Sleep Clock, Strap Options, GPIOs on Header
5. Revision History

## Adapter Board AB-88MW3XX V3.0 Schematic

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This diagram illustrates the power and module interface for the AB-88MW3XX V3.0 module, showing the connection of external components and the internal module architecture.

### Power

#### 3.3V LDO for Module

The 3.3V LDO for the module is implemented using the LT1963AES8 (U13). The input is connected to the +5V\_SYS supply through a 10µF 10V capacitor (C32). The output is connected to the +3.3V\_Module supply through a 10µF 10V capacitor (C34). The LDO is configured with a feedback network consisting of resistors R96 (6.98k 1%), R99 (5k POT), R98 (4.02k 1%), and R100 (3.6k). The LDO is also connected to the +5V\_USB supply through a 10µF 10V capacitor (C29).

#### External Battery Supply

The external battery supply is connected to the EXT\_BATTERY pin. The supply is regulated to 3.3V using a 10µF 10V capacitor (C23) and a 10µF 10V capacitor (C29). The supply is also connected to the +5V\_SYS supply through a 10µF 10V capacitor (C29).

#### 3.3V LDO

The 3.3V LDO is implemented using the MCP1824-ADJ/OT (U11). The input is connected to the +5V\_SYS supply through a 10µF 10V capacitor (C18). The output is connected to the +3.3V\_LDO supply through a 10µF 10V capacitor (C19). The LDO is configured with a feedback network consisting of resistors R75 (147k 1%) and R76 (20.5k 1%).

#### LED Power Indicator

The LED power indicator is connected to the +5V\_SYS supply through a 150Ω resistor (R92). The LED is connected to the +5V\_SYS supply through a 150Ω resistor (R92).

### Module Interface

The module interface shows the connection of the module to the external components. The module is connected to the +3.3V\_Module supply through a 10µF 10V capacitor (C29). The module is also connected to the +5V\_SYS supply through a 10µF 10V capacitor (C29).

### PIN MUXING

The pin muxing table shows the configuration of the module pins. The table lists the pin number, the pin name, and the configuration value.

Pin	Pin Name	Configuration
GPIO_24	PUSH_SW1	4
GPIO_26	PUSH_SW0	4
GPIO_34	USB_OTG_POWER_FAULT	3
GPIO_25	M_RTC_XIN	4
GPIO_22	WAKEUP0	4
GPIO_23	WAKEUP1	4
GPIO_27	USB_DRVBUS	3
GPIO_2	UART0_TXD	3
GPIO_3	UART0_RXD	3
GPIO_4	GPIO_4	3
GPIO_5	GPIO_5	3
GPIO_39	I2C0_RST	3
GPIO_40	LED1	4
GPIO_41	LED2	4
GPIO_13_M	GPIO_13	2.4
GPIO_14_M	GPIO_14	2.4
GPIO_13	GPIO_13	2.4

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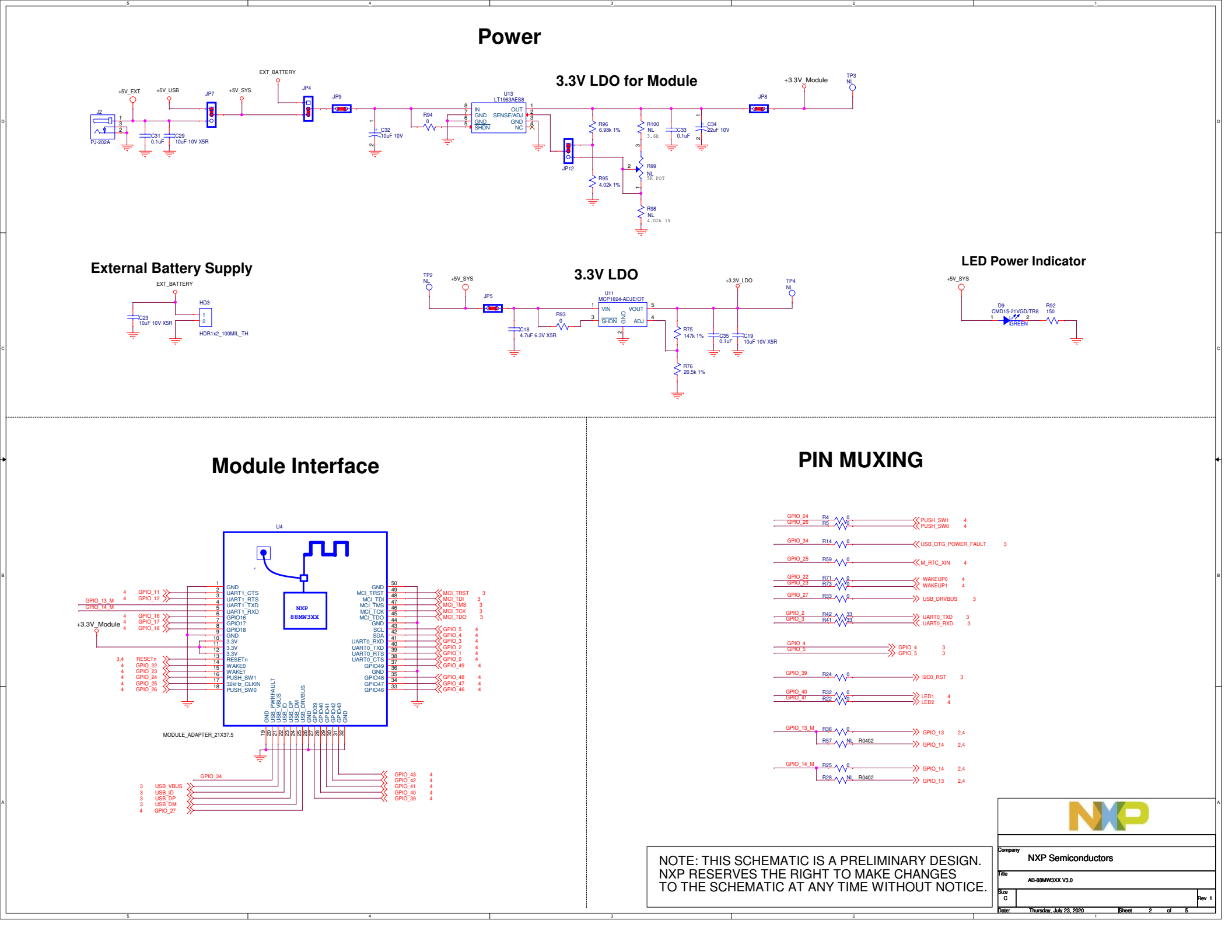
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**Power**

**3.3V LDO for Module**

**External Battery Supply**

**3.3V LDO**

**LED Power Indicator**

**Module Interface**

**PIN MUXING**

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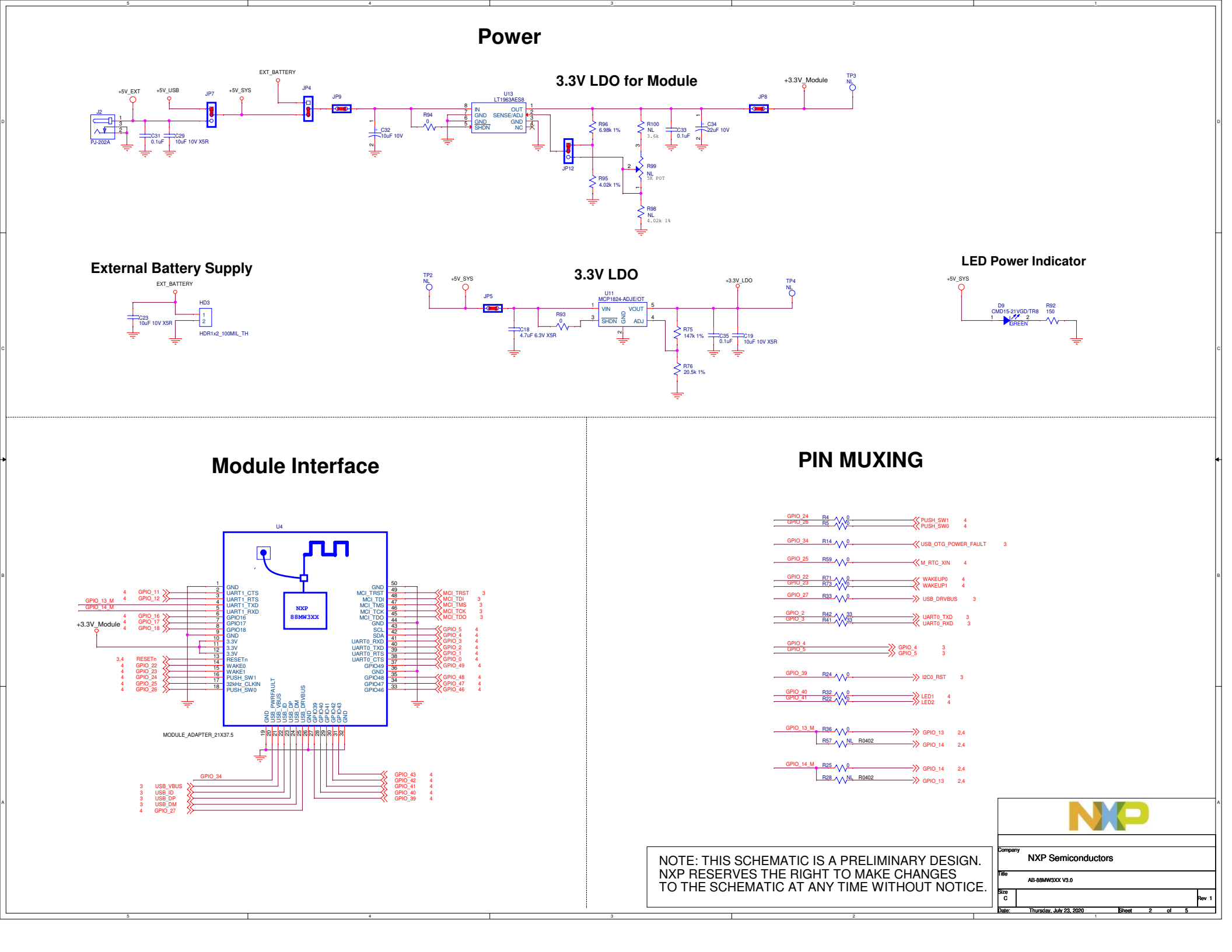
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**Power**

**3.3V LDO for Module**

**External Battery Supply**

**3.3V LDO**

**LED Power Indicator**

**Module Interface**

**PIN MUXING**

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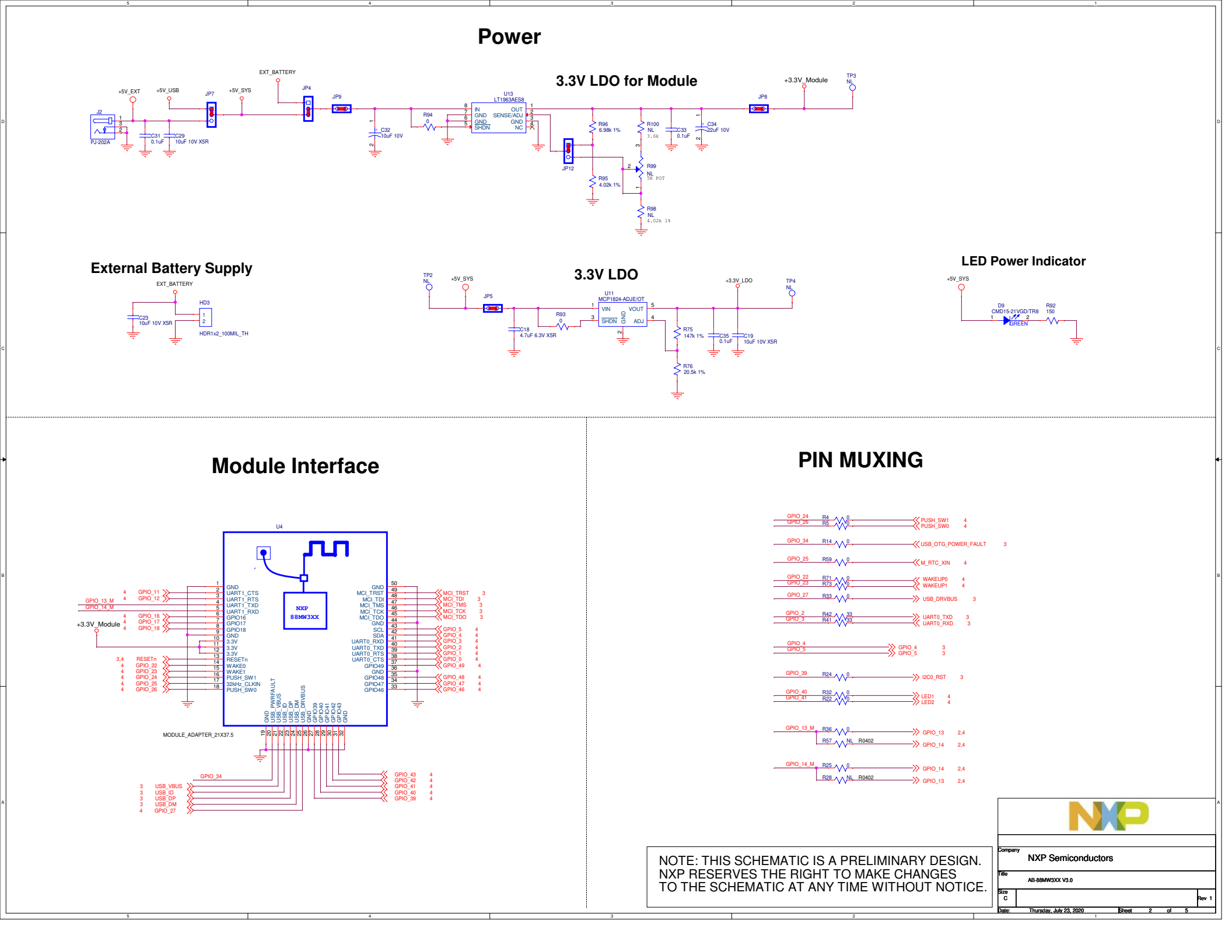
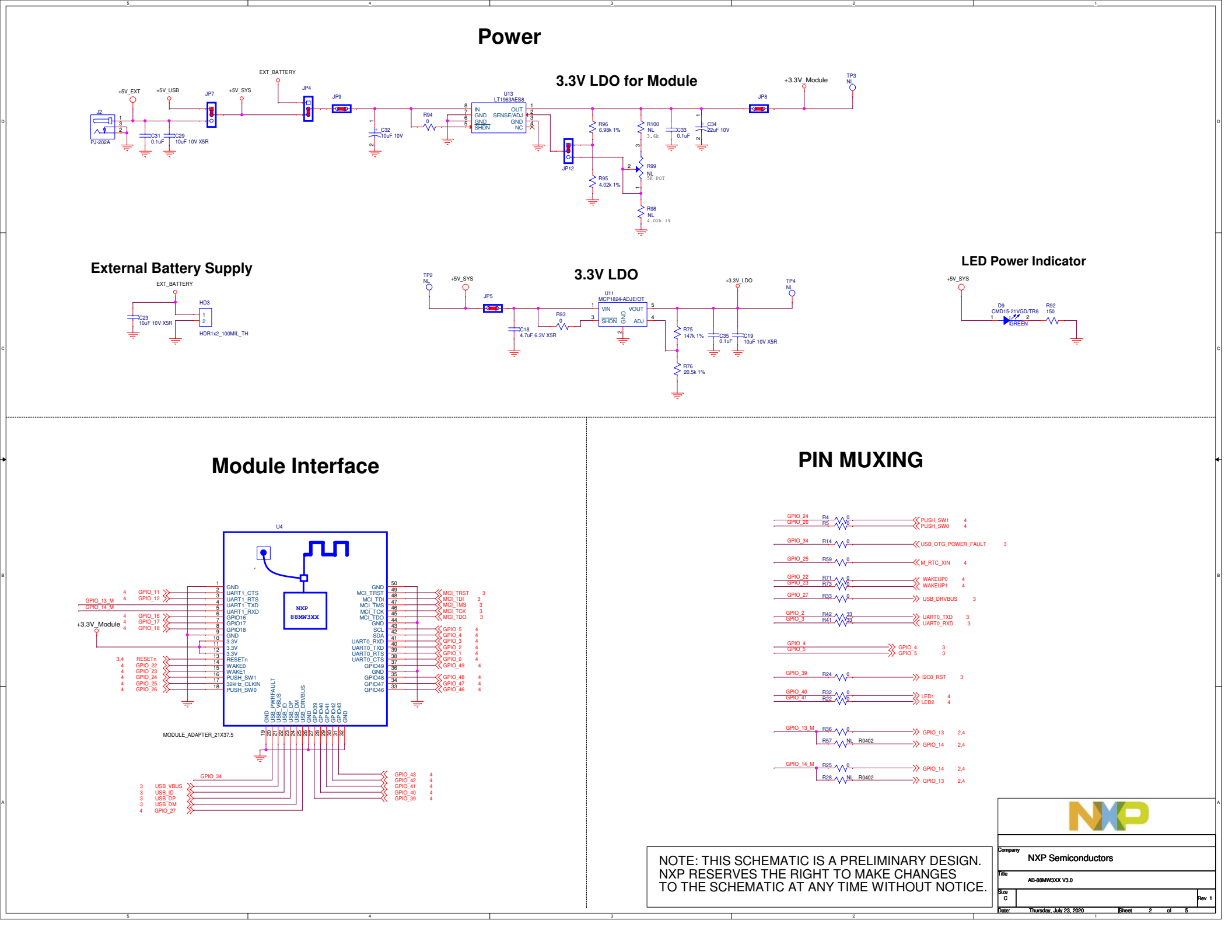
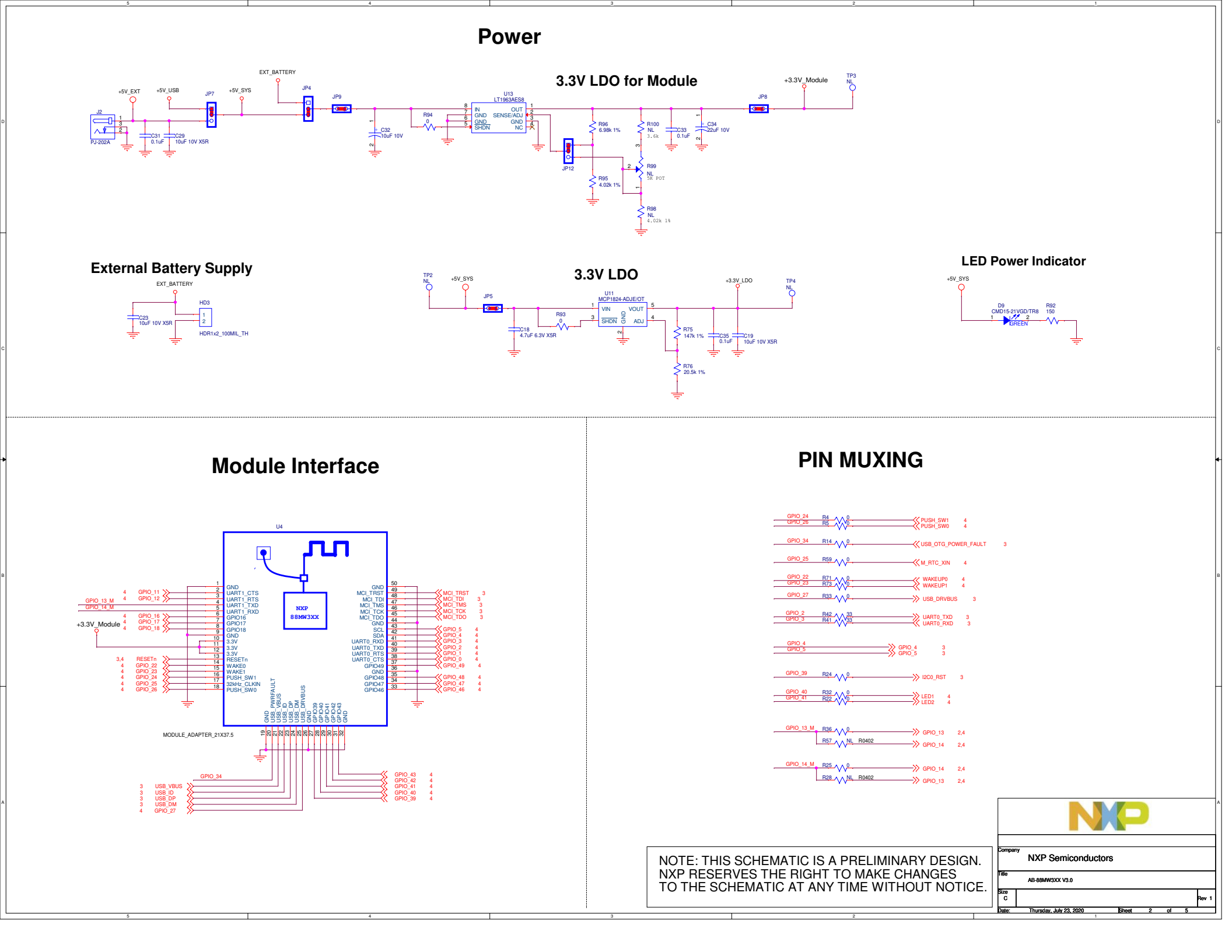
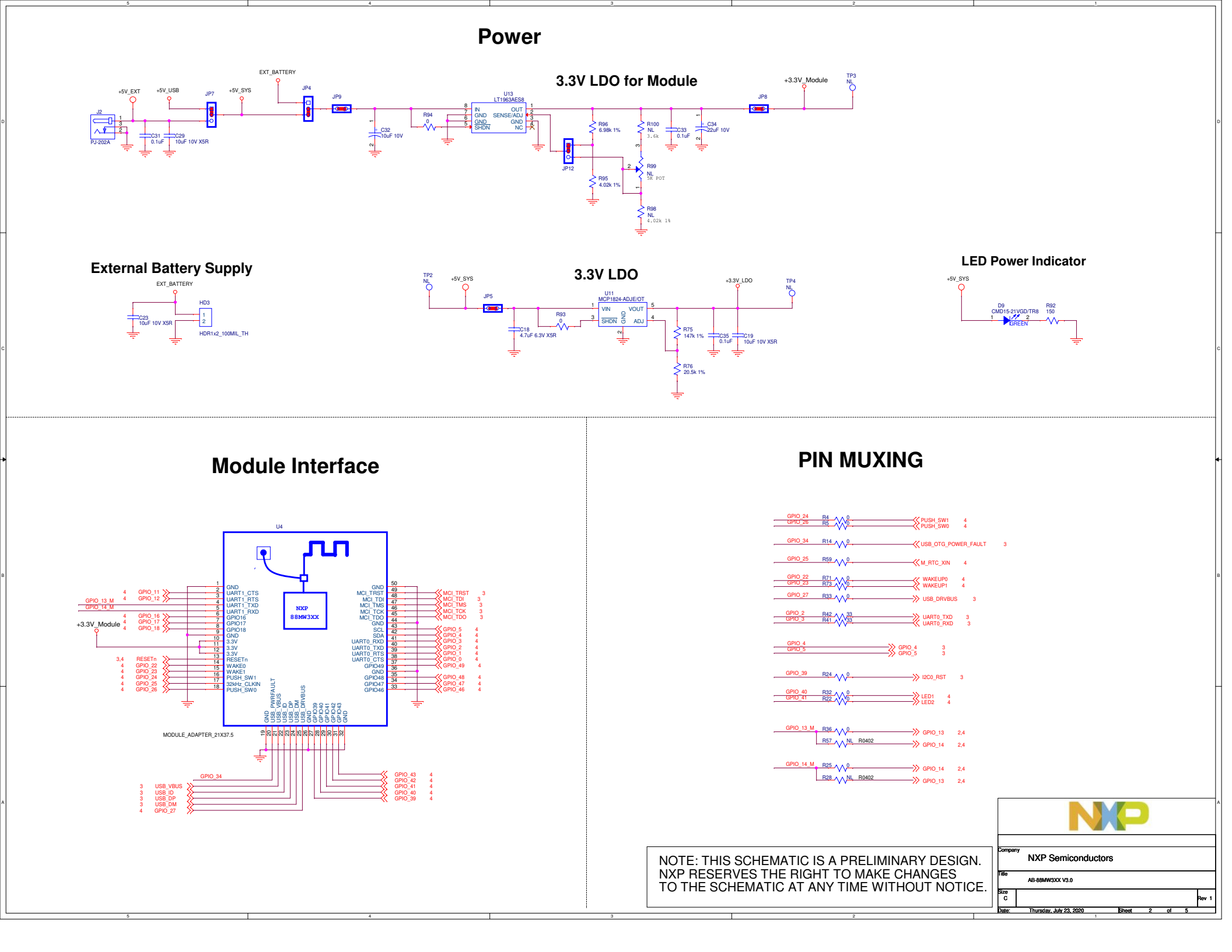
**Title** AB-88MW3XX V3.0

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**Power**

**3.3V LDO for Module**

**External Battery Supply**

**3.3V LDO**

**LED Power Indicator**

**Module Interface**

**PIN MUXING**

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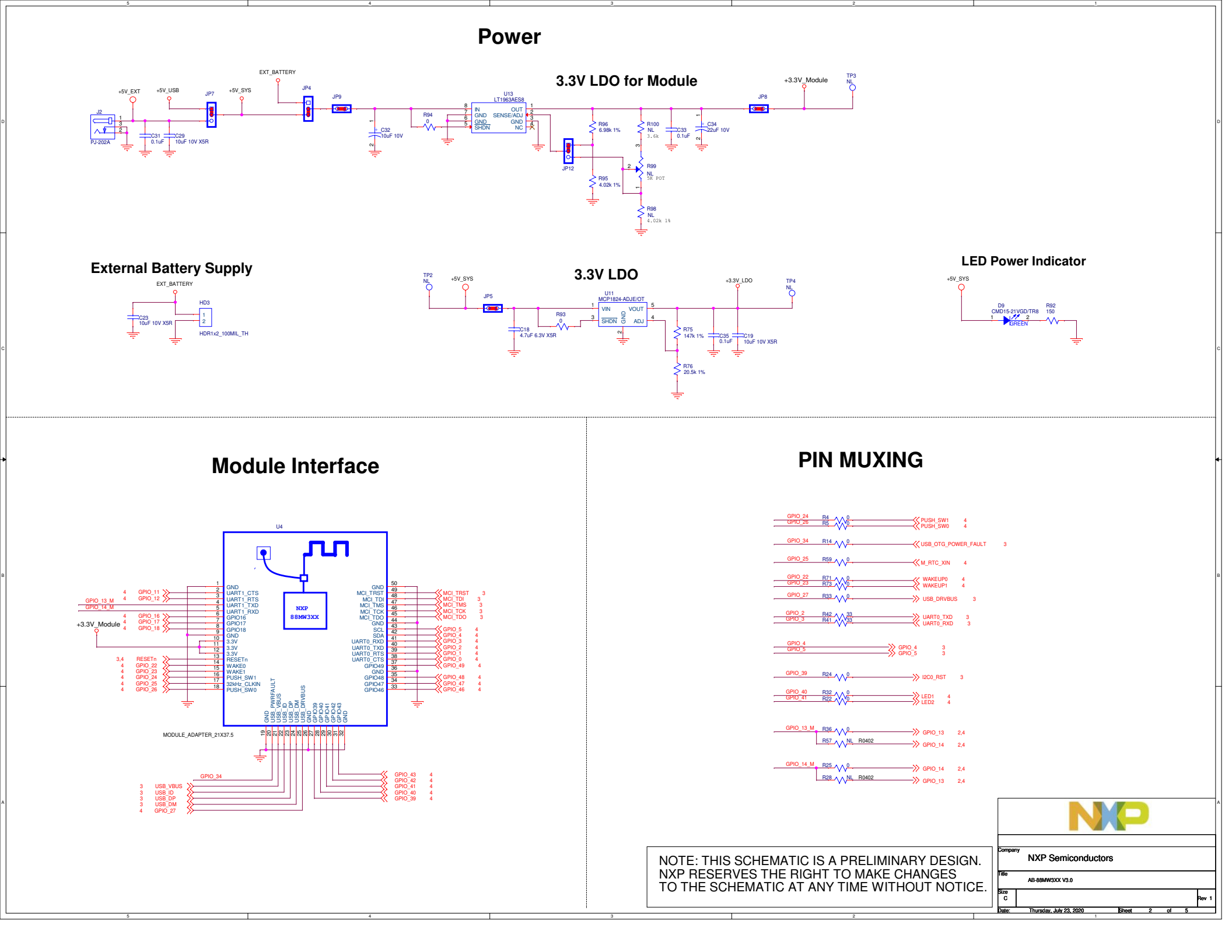
**Title** AB-88MW3XX V3.0

**Size** C

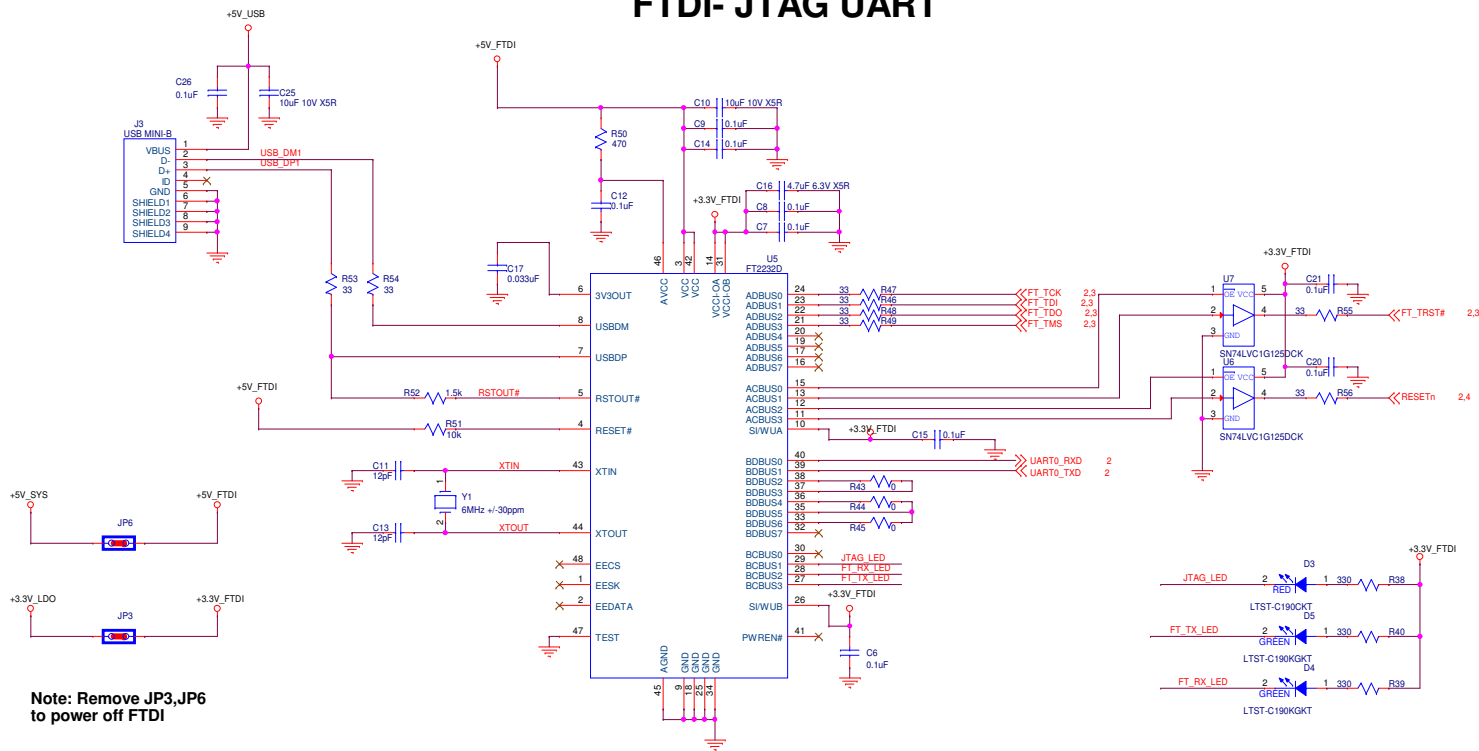
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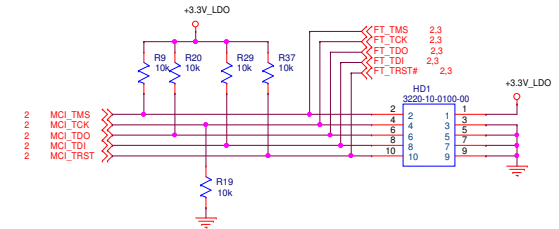
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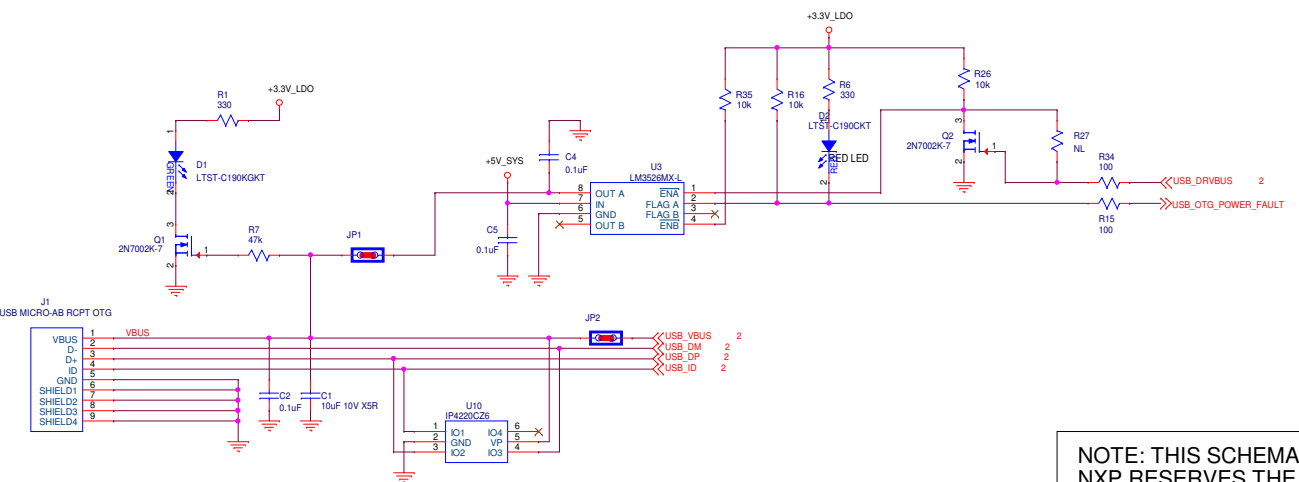
## FTDI- JTAG UART



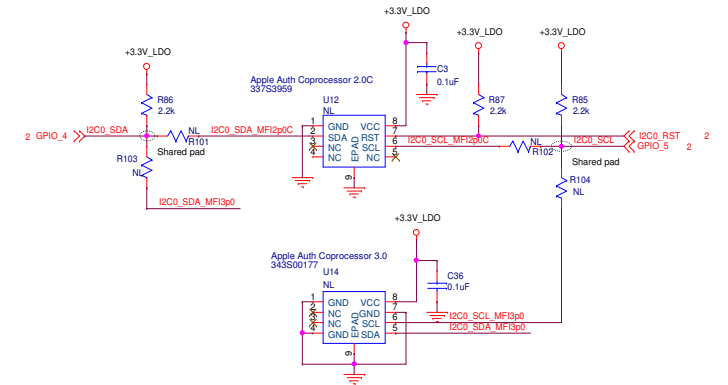
## MCI JTAG Connector



## USB OTG



## MF1 2.0C and 3.0



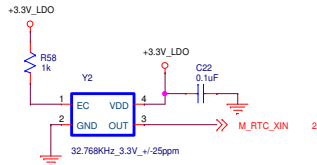
**Note:**  
Load R101 and R102 to connect I2C0 lines to MF12.0C IC ( U12)  
Load R103 and R104 to connect I2C0 lines to MF13.0 IC ( U14)  
R85, R86 = 2.2K when using MF1 2.0C ( U12)  
R85, R86 = 12K when using MF1 3.0 ( U14)

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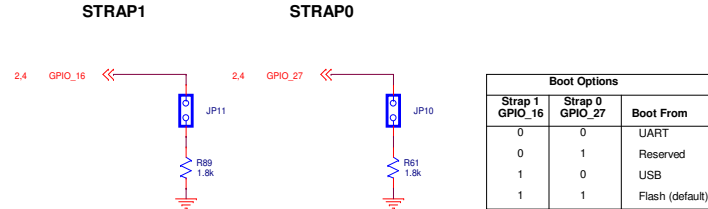


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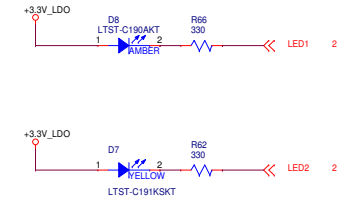
## Sleep Clock



## Strap Option



## Application LEDs

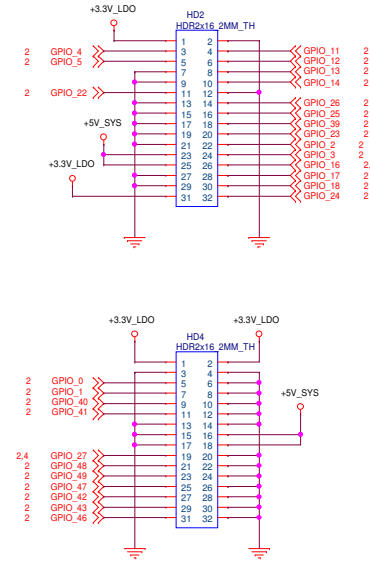


## 88MW3xx GPIOs Function Table

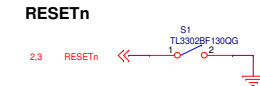
GPIO #	Function 0	Function 1	Function 2
GPIO_00	UART0_CTS	SSP0_CLK	GPT0_CH0
GPIO_01	UART0_RTS	SSP0_FRM	GPT0_CH1
GPIO_02	UART0_TXD	SSP0_TXD	GPT0_CH2
GPIO_03	UART0_RXD	SSP0_RXD	GPT0_CH3
GPIO_04	I2C0_SDA	CAN_TX	GPT0_CH4
GPIO_05	I2C0_SCL	CAN_RX	GPT0_CH5
GPIO_11	UART1_CTS	SSP1_CLK	IR_IN
GPIO_12	UART1_RTS	SSP1_FRM	IR_OUT
GPIO_13	UART1_TXD	SSP1_TXD	IR_TXM
GPIO_14	UART1_RXD	SSP1_RXD	—
GPIO_16	STRAP1	—	—
GPIO_17	GPT3_CH0	I2C1_SCL	—
GPIO_18	GPT3_CH1	I2C1_SDA	—
GPIO_22	WAKE0	—	—
GPIO_23	WAKE1	—	—
GPIO_24	PUSH_SW1	GPT1_CH5	—
GPIO_25	32KHz_CLK_IN	I2C1_SDA	CAN_TX
GPIO_26	PUSH_SW0	I2C1_SCL	CAN_RX
GPIO_27	STRAP0	USB_DRVBUS	—
GPIO_34	USB_PWR_FAULT	—	—
GPIO_39	I2C0_RESET	IR_IN	—
GPIO_40	LED1	IR_OUT	—
GPIO_41	LED2	IR_TXM	—
GPIO_42	ADC0_0	ACOMP0	VOICE_P
GPIO_43	ADC0_1	ACOMP1	VOICE_N
GPIO_46	SSP2_CLK	UART2_CTS	ADC0_4
GPIO_47	SSP2_FRM	UART2_RTS	ADC0_5
GPIO_48	SSP2_TXD	UART2_TXD	ADC0_6
GPIO_49	SSP2_RXD	UART2_RXD	ADC0_7

(NOT ON HEADER)

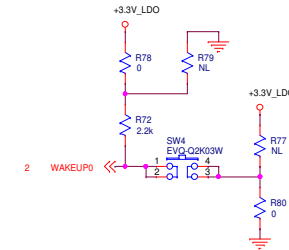
## GPIOs on HEADER



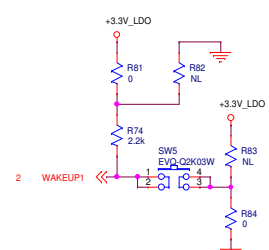
## Push Buttons



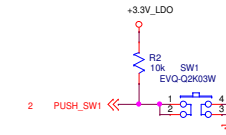
### WAKE0



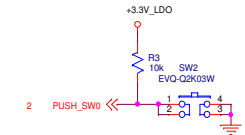
### WAKE1



### PUSH BUTTON 1



### PUSH BUTTON 2



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REVISION HISTORY

Design Version	Document Revision	Date	Change List
V 3.0	Rev 1	31-Jul-2020	Initial Release

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